AGENDA

PAGE 0 – CONFERENCE & WORKSHOPS DAY; PAGE 1,2,3 – TRAINING DAYS

DATA AREA – AREA WHERE YOU RECEIVE DATA

SPARE AREA – AREA WHERE YOU RESET

ECC AREA – AREA WHERE YOU PROCESS DATA, ASK QUESTIONS AND DO CORRECTIONS

TIMELINE OFFSET 0009h

PAGE 0 - MAY 7

09:00 REGISTRATION

000Ah 10:00 INTRO

eMMC-NAND RECONSTRUCTOR FUNDAMENTALS

COFFEE BREAK & QUICK WORKSHOP

000Bh 11:00 eMMC-NAND RECONSTRUCTOR CASE STUDY

BREAK & QUICK WORKSHOP

000Ch 12:00 NEW FILE CARVER CASE STUDY

BREAK & QUICK WORKSHOP

000Dh 13:00 LUNCH

000Eh 14:00 MODERN DIGITAL FORENSIC CHALLENGES AND BELKASOFT APPROACH IN SOLVING THEM BELKASOFT

COFFEE BREAK & QUICK WORKSHOP

000Fh 15:00 VNR SQLITE CARVER CASE STUDY

BREAK & QUICK WORKSHOP

0010h 16:00 SPARE AREA XOR KEY EXTRACTION CASE STUDY

BREAK & QUICK WORKSHOP

0011h 17:00 NEW READ RETRY CASE STUDY

BREAK

0012h 18:00 DIGITAL FORENSICS & AUTOMOBILE ELECTRONICS UNIVERSITY OF SOUTH WALES

18:30 COFFEE BREAK & QUESTIONS AND ANSWERS

0013h 19:00

CONFERENCE DAY

TRAINING DAYS

PAGE 1 - MAY 8

TRAINING

COFFEE BREAK

TRAINING

LUNCH

TRAINING

COFFEE BREAK

TRAINING

QUESTIONS & ANSWERS

PAGE 2 - MAY 9

TRAINING

COFFEE BREAK

TRAINING

LUNCH

TRAINING

COFFEE BREAK

TRAINING

QUESTIONS & ANSWERS

18:30 BARBEQUE PARTY

PAGE 3 - MAY 10

TRAINING

COFFEE BREAK

TRAINING

LUNCH

TRAINING

COFFEE BREAK

TRAINING

THE END

QUESTIONS & ANSWERS

CHIP-OFF WEEK 2019

TRAINING AGENDA

Module 1: FLASH MEMORY USAGE OVERVIEW
Overview
Diversity of devices
Structure, components and functionality
Standard and monolithic devices
Controller and NAND memory functions
Typical damages and problems of flash memory devices
Chip-off solution
Data recovery workflow

Module 2: NAND FLASH MEMORY
NAND memory packages
NAND interface
Internal structure
Crystals, Planes, Blocks, Pages
Data allocation within memory
NAND parameters
Direct memory access mode
Bit errors in NAND memory
Voltage tuning for better reading
Physical image extraction

Module 3: PHYSICAL IMAGE OF NAND MEMORY
Internal structure
Blocks, Pages, Data, Spare and ECC areas
Page layout
Spare area structure

Module 4: FLASH CONTROLLERS
Data flow from interface to NAND
Block management, wear leveling and translation
Single plane/Multi plane page allocation
Data optimization in controller's channel
Encryption
Inversion
Scrambling
Error Correction Codes
Page shaping

Module 5: REVERSE OPERATIONS (steps of reconstruction)
Page layout
ECC correction
Inversion
Descrambling
Page allocation analysis
Block management

Module 5: VISUAL NAND RECONSTRUCTOR
Software overview
Database, settings and components
Workspace overview
Elements, Parameters, Toolbars and functions
Dump viewers
Hex, Bitmap, Structure viewer
Bitmap concept
Work in Bitmap and Structure viewer

Module 6: PHYSICAL IMAGE ANALYSIS BASED ON PATTERNS
Page layout analysis
LAB: Page structure analysis on 2-4 dumps
Data, Spare and ECC area patterns
LAB: ECC detection on 2-3 cases
Inverted data patterns
LAB: Analysis of inversion on 1-2 cases
Scrambled/Non-scrambled data patterns
LAB: Analysis of scrambler and XOR key on 2-3 cases
Page allocation patterns
LAB: Page allocation analysis on 2-3 cases

Module 7: BLOCK TRANSLATION ALGORITHM
Concept of block management and translation
Block size determination
Spare area pattern analysis
Logical Block Number parameters
Header parameters
Translator creation in software
Missing and duplicated blocks
Logical image creation

Module 8: LOGICAL IMAGE RECONSTRUCTION PROCESS
Three phases of the data recovery process
Physical images
Virtual images
Logical image
Translator adjustment
Analysis of conflicts within block sequence

Module 9: PRACTICAL DATA RECOVERY ON DUMPS
LAB: Low complexity 2-3 cases
LAB: Medium complexity 2-3 cases
LAB: High complexity 1-2 cases

Module 10: PRACTISE WITH NON-STANDARD AND COMPLICATED CASES
Bad columns
Analysis and removal
LAB: Data recovery with bad columns on 1 case