

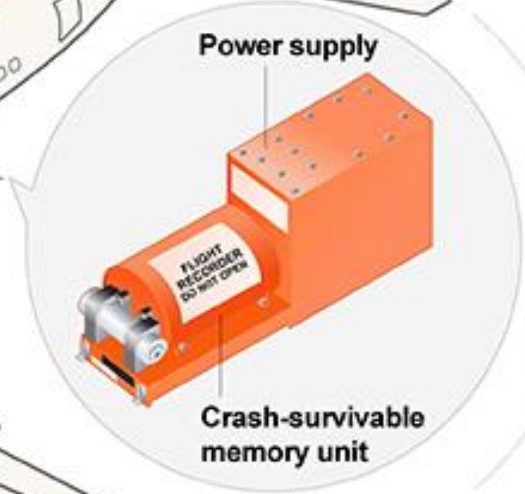
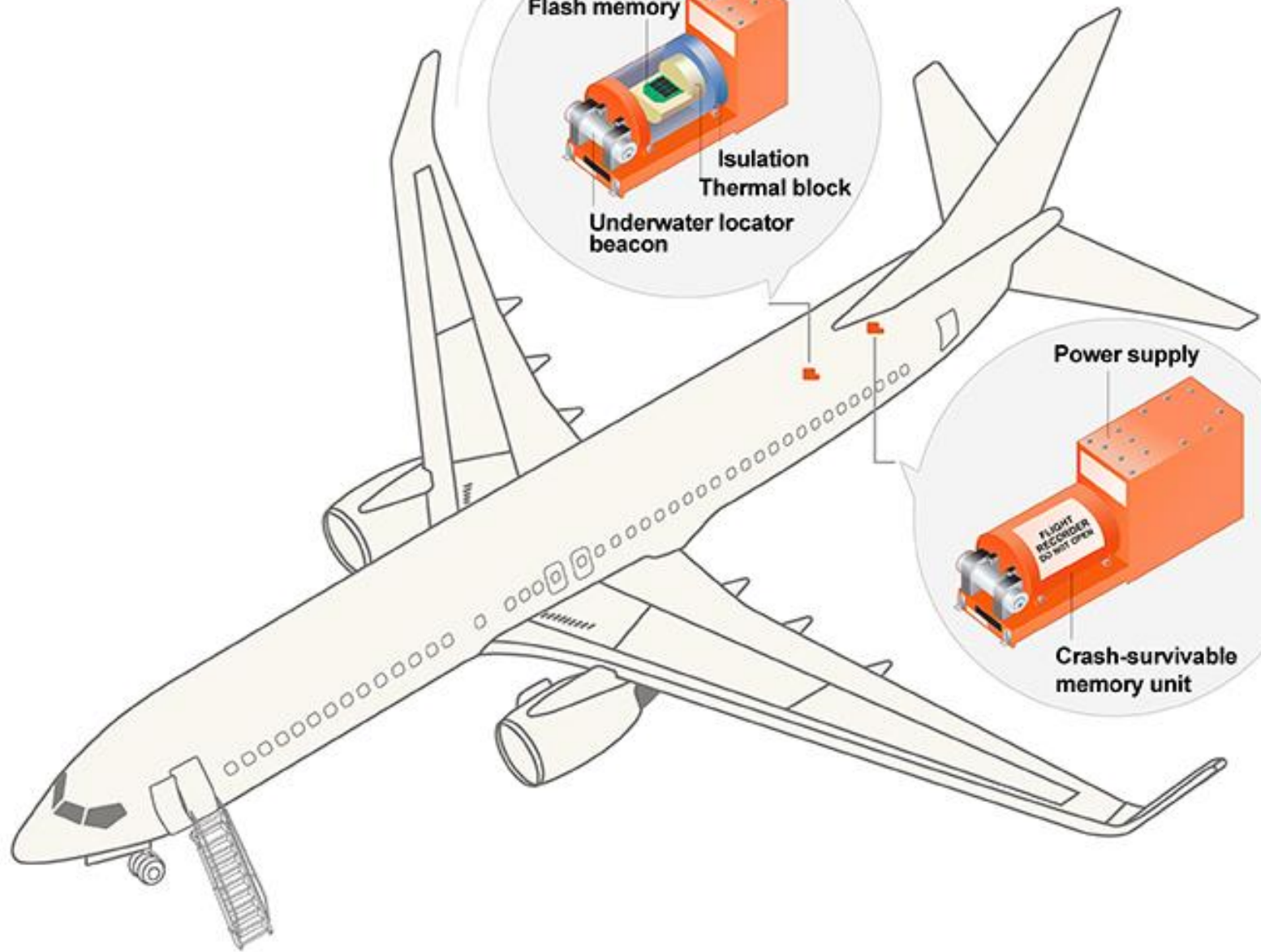
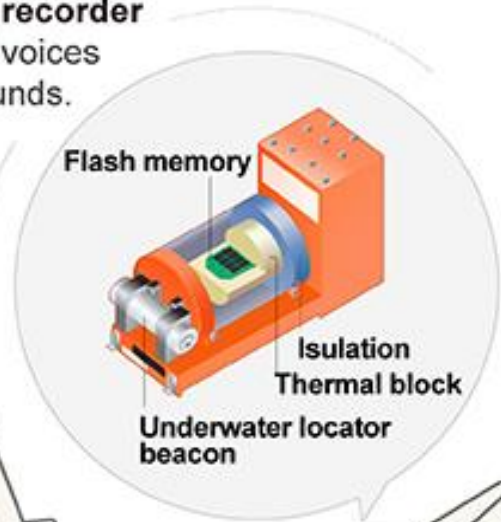
Flash memory technology in Aircraft Black boxes. Data recovery case studies.

Michał Gmurek, Rusolut

Data Recovery from Aircraft Black Box



Cockpit voice recorder
preserves pilot voices
and cockpit sounds.



Flight data recorder
captures such
information as altitude,
airspeed, heading and
engine thrust.

D.T.MUX Sentinel™



Crash Protected System
from 32 to 128GB



Reference#

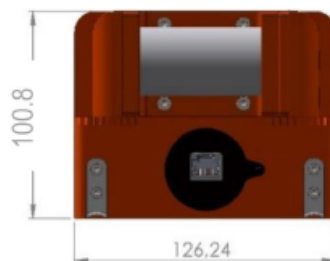
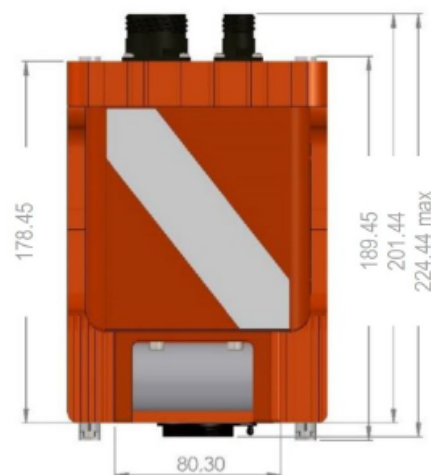
SEN-XXX





MECHANICAL

	Specification	Remark
Size	189.5 (231.8 iRIPS / 219.5 iEE) x 126.2 x 101 mm	D x W x H ± 1mm
Weight	≈ 3.30kg / 3.75kg ≈ 4.85kg	ED155/ ED112 iRIPS
Connectors	MIL-DTL-38999	Serie III
Mounting	ARINC 404	Customizable



ELECTRICAL

Input Voltage	28Vdc (16 to 36Vdc)
Power consumption	≈ 12 to 32 watts (28Vdc)
Power Interruption	≈ 200 to 800ms
Standard	MIL-STD-704F / DO-160

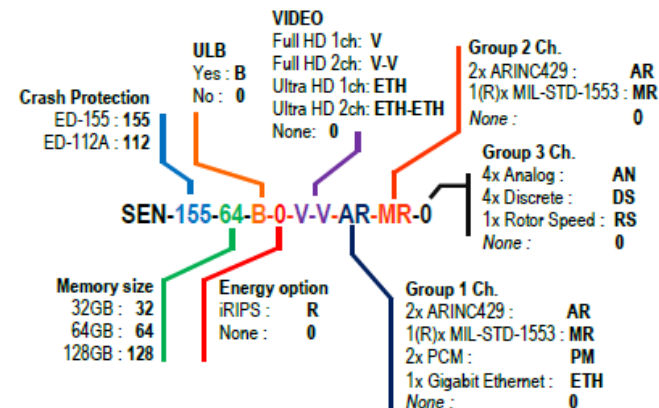
ENVIRONMENTAL

	Specification	Remark
Temperature	-40°C to 65°C -55°C to 90°C	Operating Storage
Cooling	Passive	Convection
Humidity	95%	Non-Cond
Vibration	5Hz to 2KHz	6.29 g RMS
Shocks	20g 11ms	Operating
Acceleration	20g linear 3 axis	Operating
Altitude	+ 60,000 ft	Operating
Decompression	420Kpa/minute	Operating
MTBF	> 90,000 hours	Computed
EMI	DO-160	Rev G

STANDARD FUNCTIONALITY

	Specification
Gigabit	Configuration/Control
Ethernet	Data download and Streaming
Time synch	GPS Antenna input / Irig B / PTP v2
Voice	4x Audio channels
Recording	IRIG 106 Chapter 10 / DTMUX format
Sensors	Internal 3 Axis Gyro/ G force/ Pressure
COM port	RS-232 Configuration/Maintenance
Status	Status Led / Status output

SENTINEL PART NUMBER COMPOSITION



Environmental specifications

Environmental specifications

The equipment has been designed to meet the environmental specifications applicable to the installation limits as set forth in the version of RTCA/DO-160 in force at the time of certification.

Flight Recording Systems (ED-112), Survivability

- Impact: 3400 Gs, 6.5ms, All Axes
- Pin Penetration: 500 lb., 10 ft. (1/4 in. Pin)
- Static Crush: 5000 lb, 5 min All Axes
- Low Temp Fire: 260°C, during 10 hours
- High Temp Fire: 1,100°C, during 60 Min
- Sea Water Immersion: 30 Days
- Deep Sea Pressure: 20,000 ft., 24 Hrs.
- Fluid Immersion: Various Fluids, 48 Hrs.

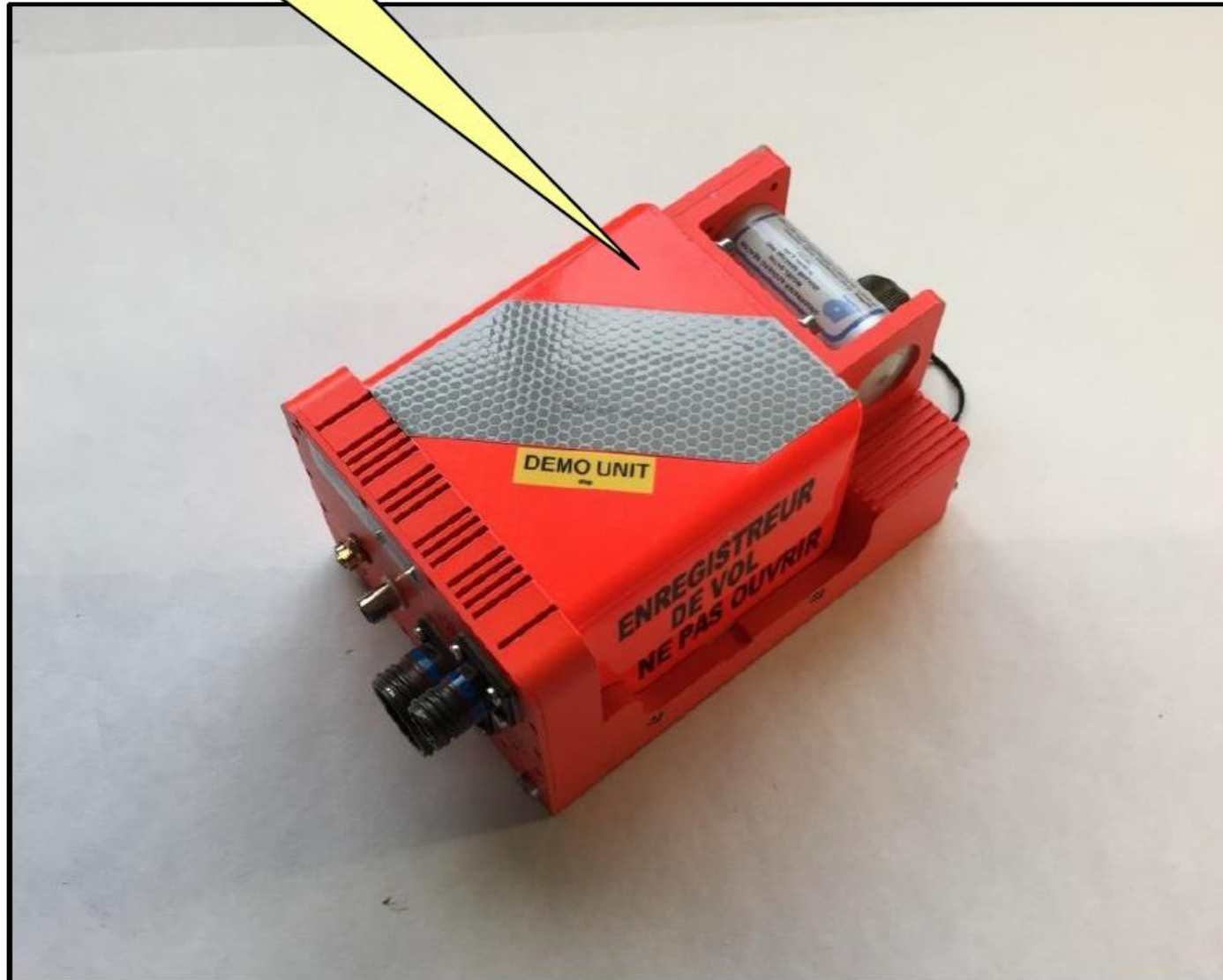
Qualification/Certification

Sentinel "ED-112 type" meets the requirements as specified in the Minimum Operational Performance Specification (MOPS) for flight recording systems ED-112. The system also outperforms many of the crash survival requirements in the Minimum Operational Performance Specification for Crash Protected Airborne Recorder Systems ED-112.

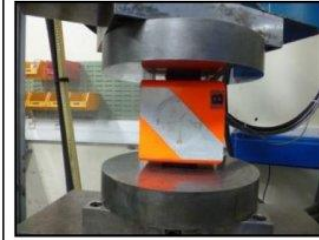
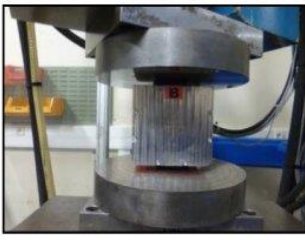


Sentinel Under High temperature fire test

Crash Protected
Memory Block



Hydraulic press test



Diagonal 1



Diagonal 2

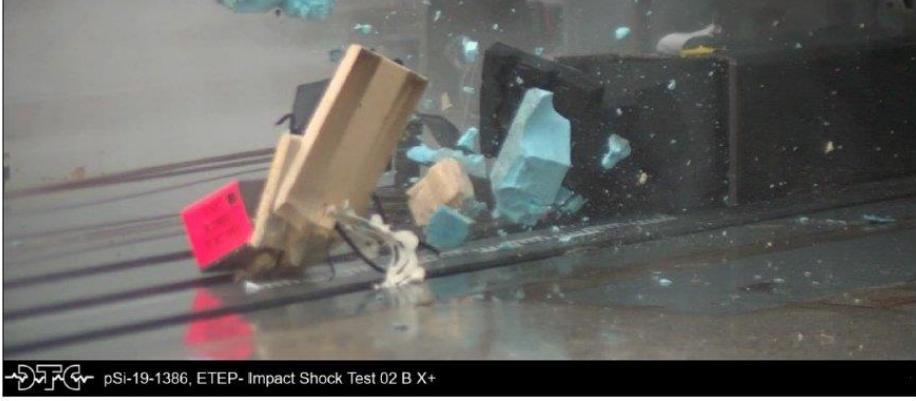


Diagonal 3

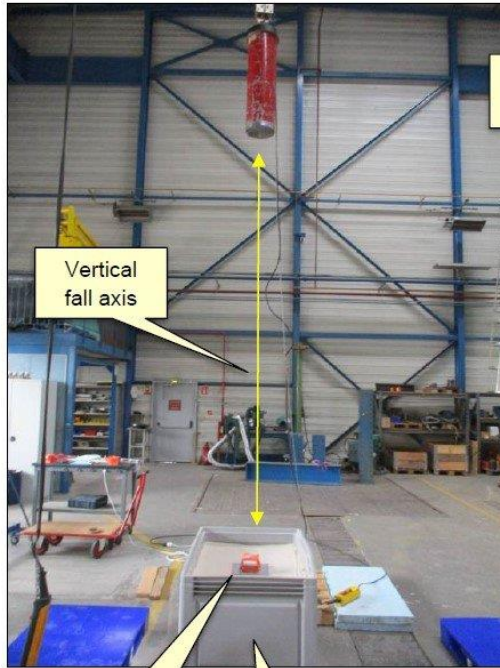


Diagonal 4

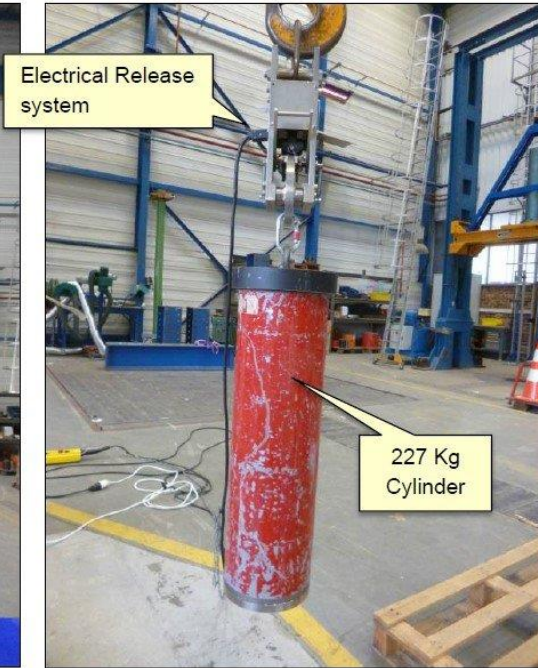
Crash test



Impact test



Vertical fall axis



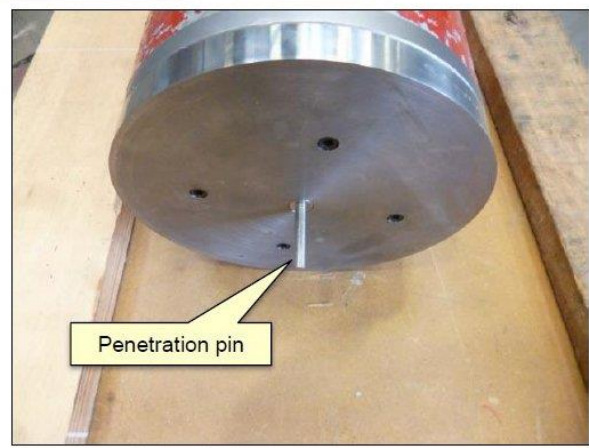
Electrical Release system

227 Kg Cylinder



Sentinel CSMU

Sandbox



Penetration pin



Steel plate



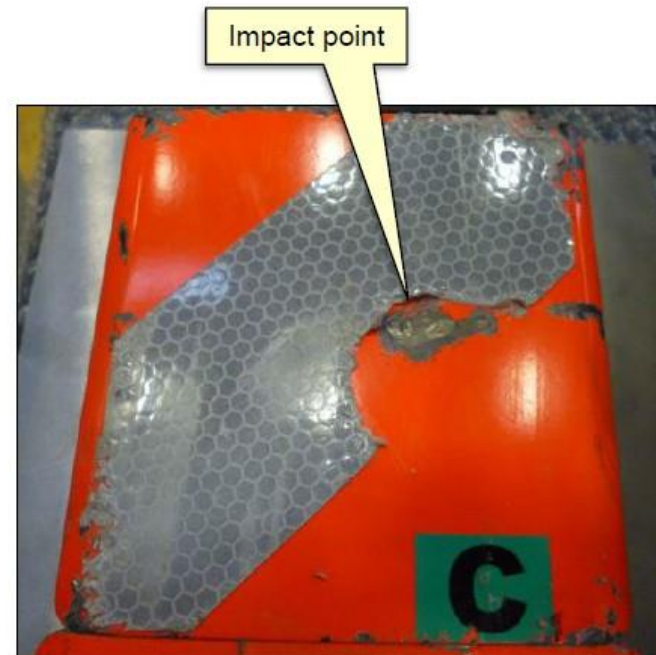
Mechanical crash test results



CSMU "A", "B" and "C" has successfully pass test sequence, no penetration or deformation of structure has been noted for each one.

Note:

Data contained inside robust memory are not analyzed before end of test sequence.





IFREMER is a French institute that undertakes research and expert assessments to advance knowledge on the oceans and their resources, monitor the marine environment and foster the sustainable development of maritime activities.

For more information consult Ifremer website:
<https://wwz.ifremer.fr/en/>

The Sentinel CPM is placed in hyperbaric chamber during 24 hours at 625 Bar, in saltwater to simulate a depth of 6000m. The materials used to protect the recording medium have been shown to be unaffected by sea water (Titanium ...)



High pressure test

Sentinel CSMU Structure



This test must determinate if the crash protected memory Sentinel can resist to an equivalent depth of 6 000 m (20 000 feet).

We no detected any change of the Sentinel CPM structure after 24 hours at 625 Bar.

After this test in laboratory we don't note any deformation of the structure, and the structure is remains in **full integrity**.



High temperature test



Test has been conducted on Crash Protected memory unit destined to equip Sentinel System. The fire test is started by turning on the main gas valve. Flame temperature, as indicated by the external thermocouples, is continuously monitored. Figure 2 picture show Crash Protected Memory module under high temperature test.

At the end of the test period, the burners have been shut off and the robust memory module has been cool naturally in ambient conditions. The crash Protect memory unit has been removed from the vicinity of the support arrangement.

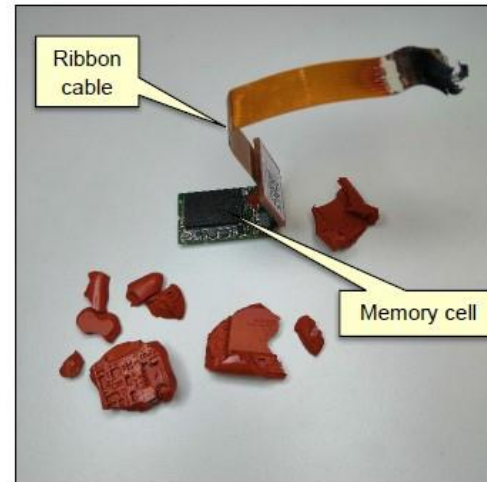
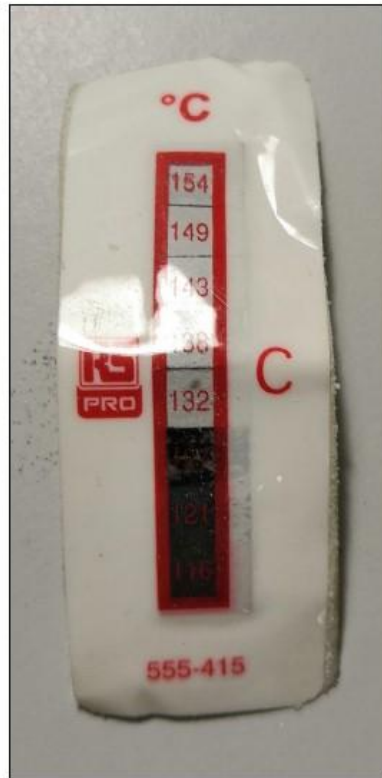
High temperature test results



The unit is progressively put back to room temperature (natural cooling) the time is approximatively 3 hours before being able to go for opening process.

we don't notice any deformation of the structure and the structure is in **full integrity**. Bright orange paint has disappeared.

Reached temperature inside enclosure up to 132°C



After the test sequence has been performed, this test pattern shall be readily recoverable to establish that the bit error rate defined in Chapter 2-4 has not been exceeded.

After this test the Sentinel crash protected memory is open to verify if the PCB did not damaged and if the data is still readable. After remove of all insulation protection (Ceramic, white powder material and red silicon protection), we examine the memory PCB.

Solid state drive integrity

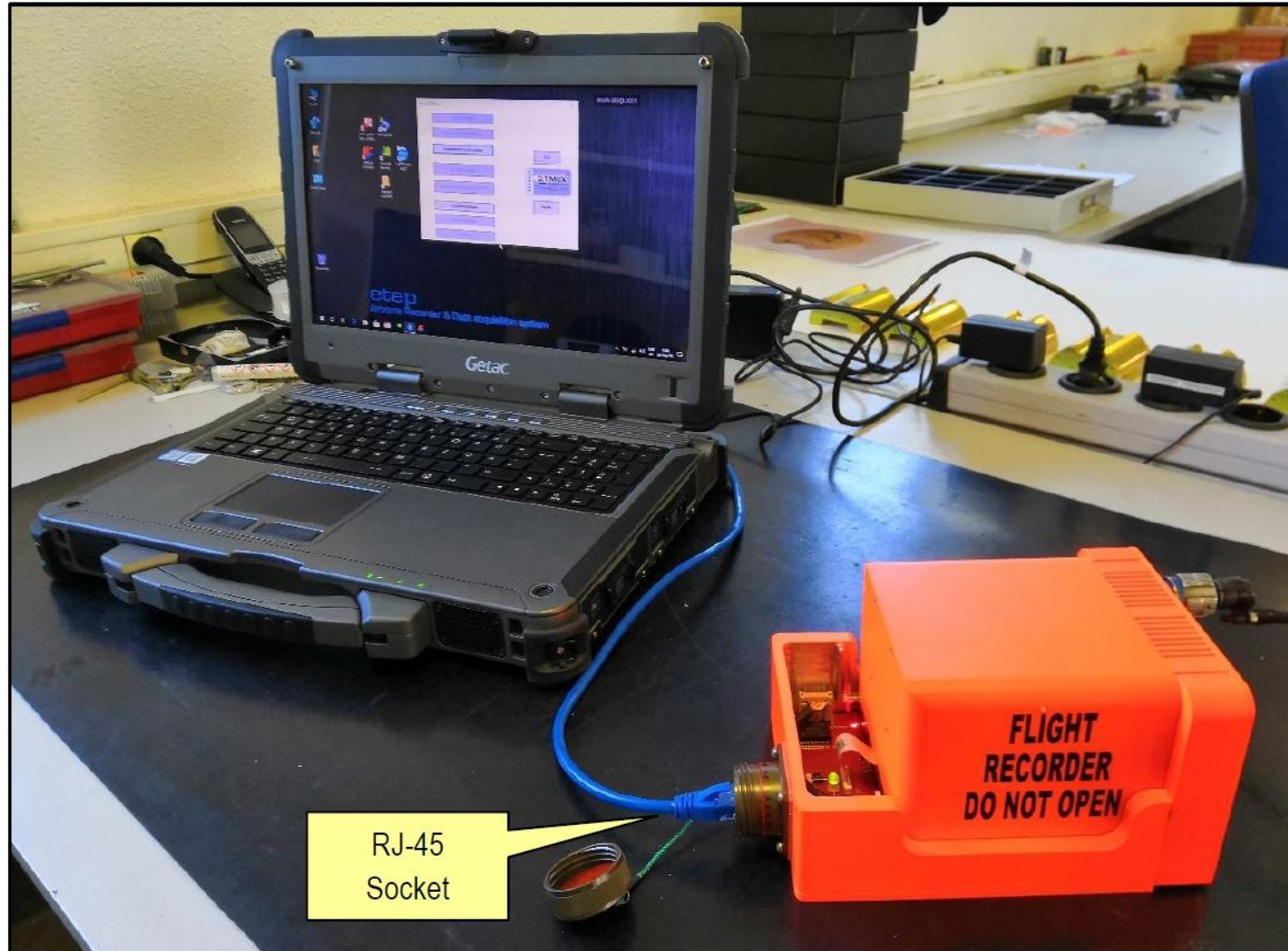
After a visual inspection, we no detect any damages on solid state drive circuit.

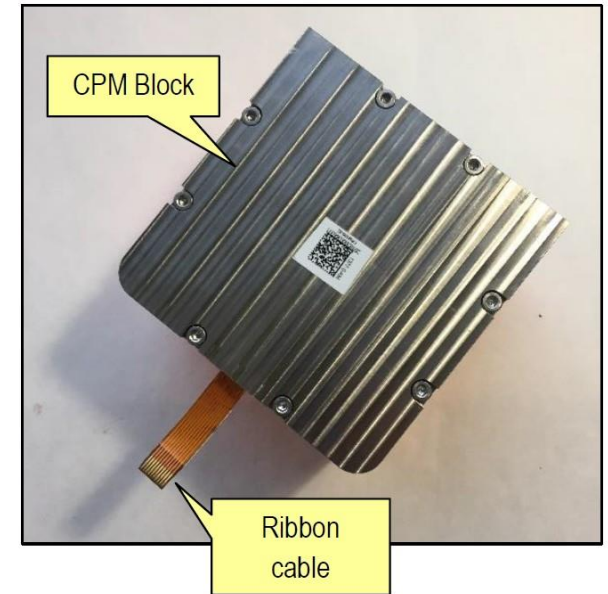
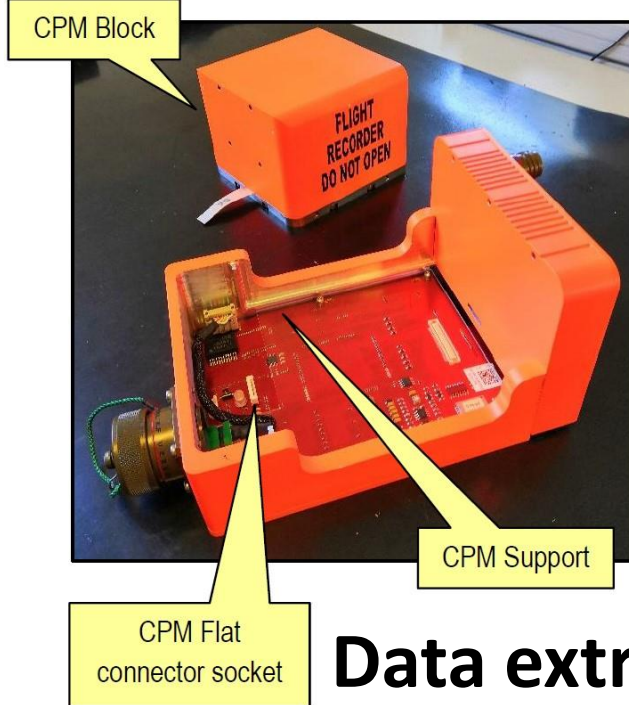
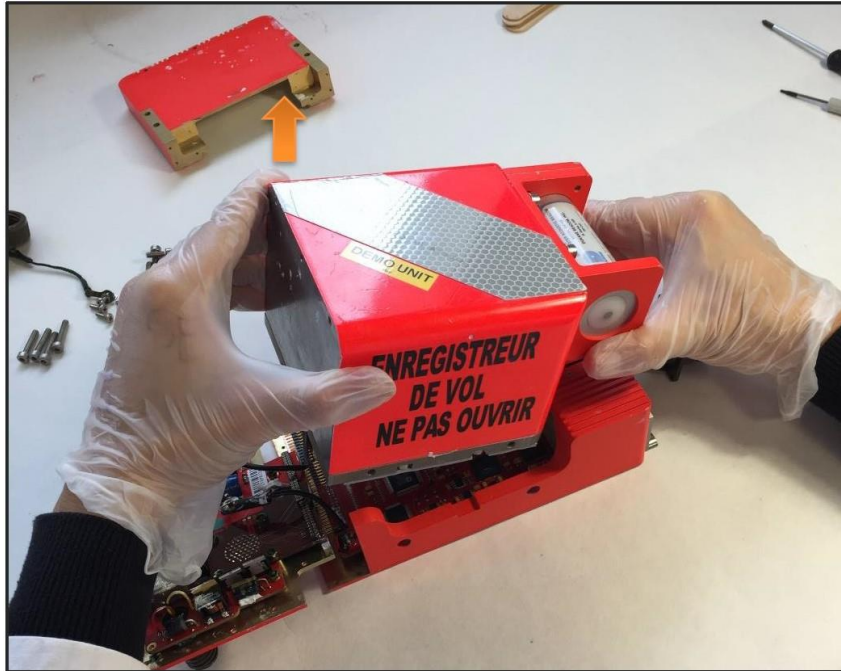
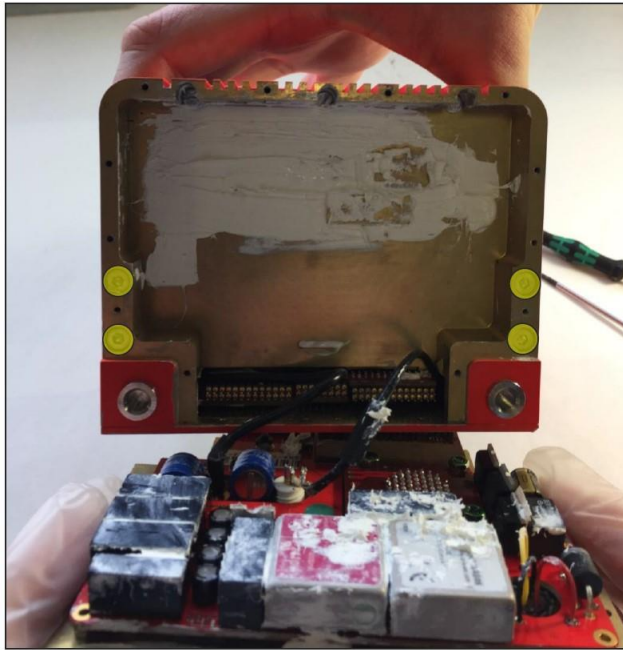
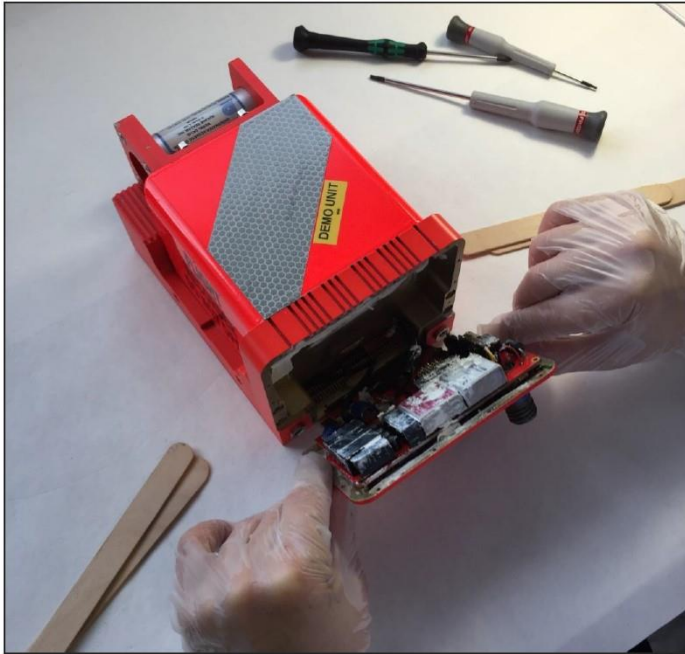
The memory unit was tested to verify if the data is in full integrity.

The data is in full integrity and no present any error.

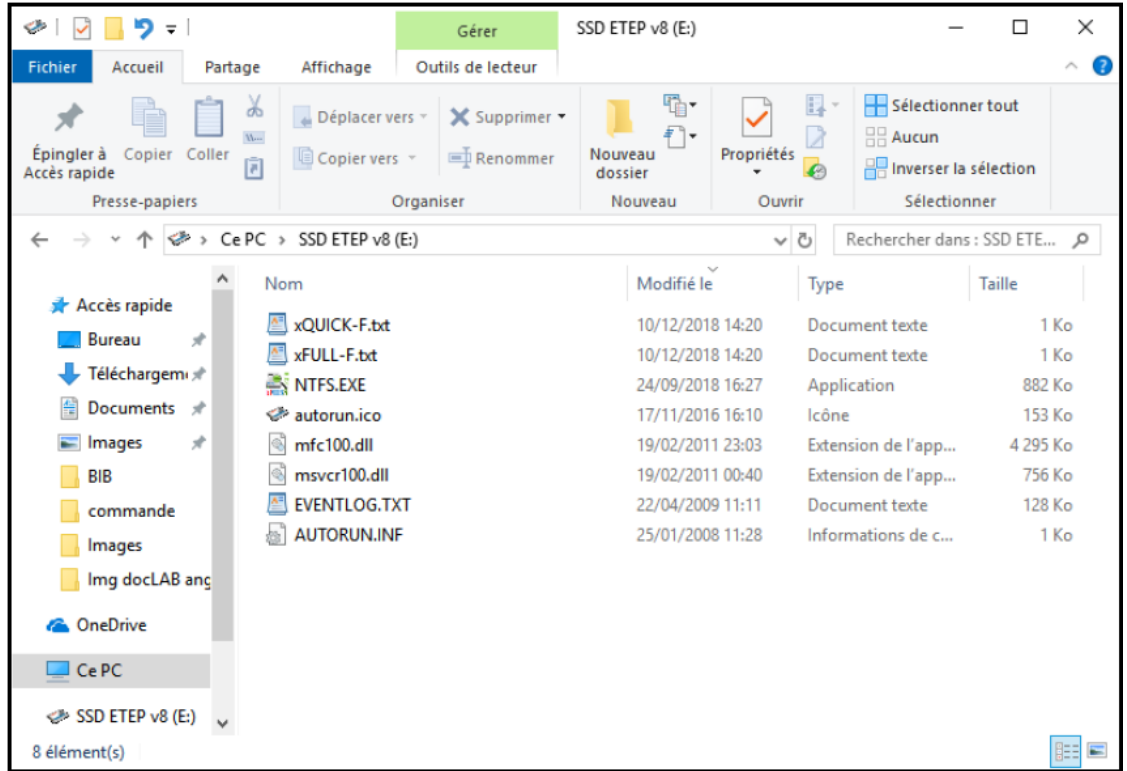
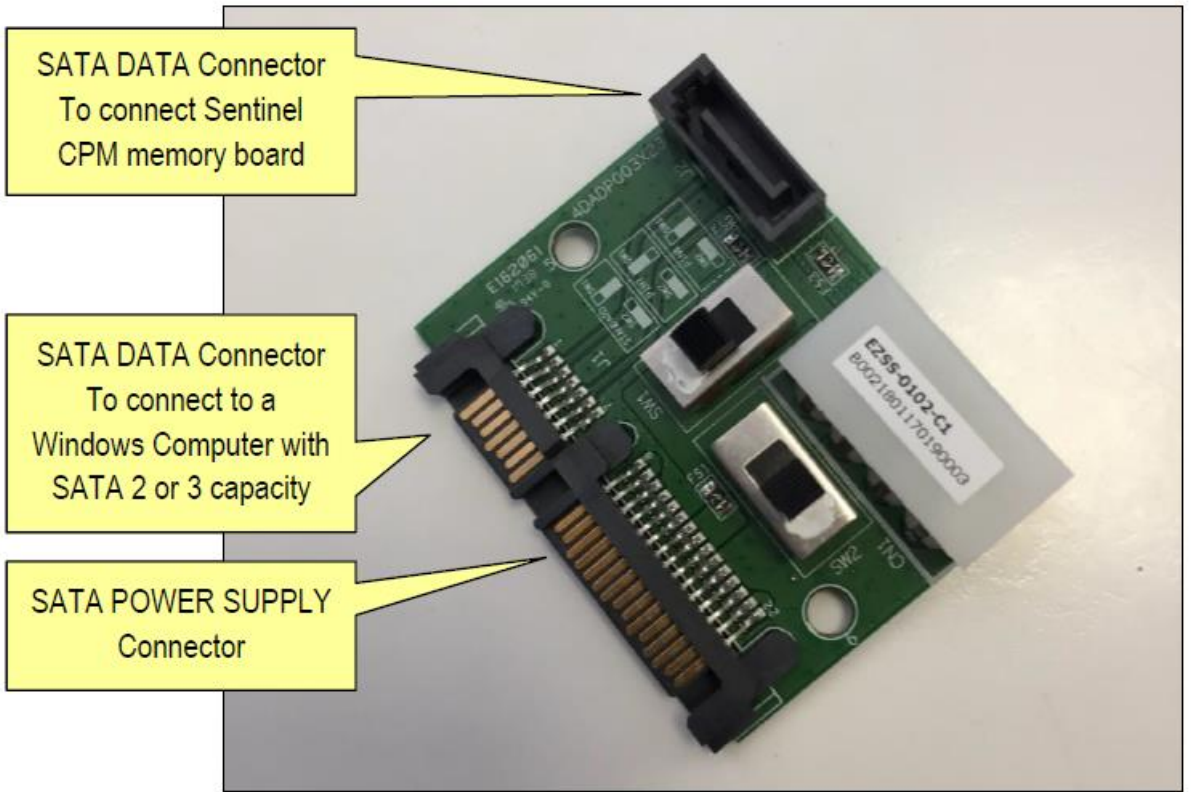


Data extraction via external interface





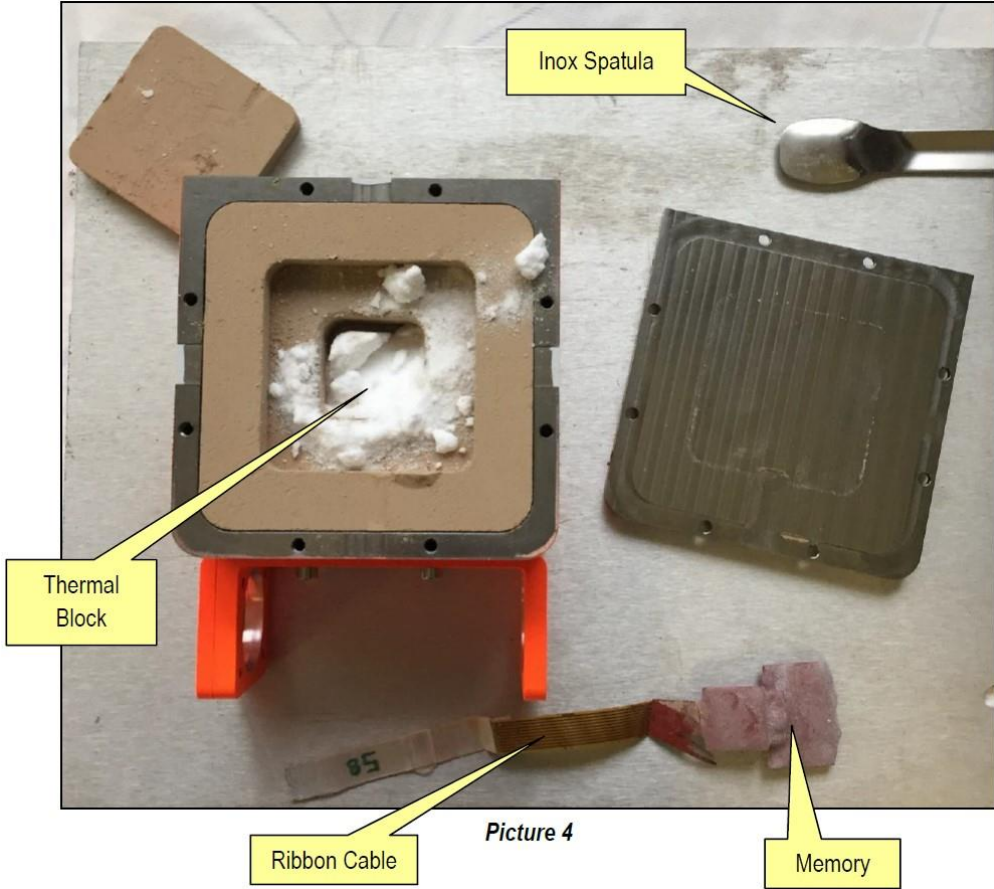
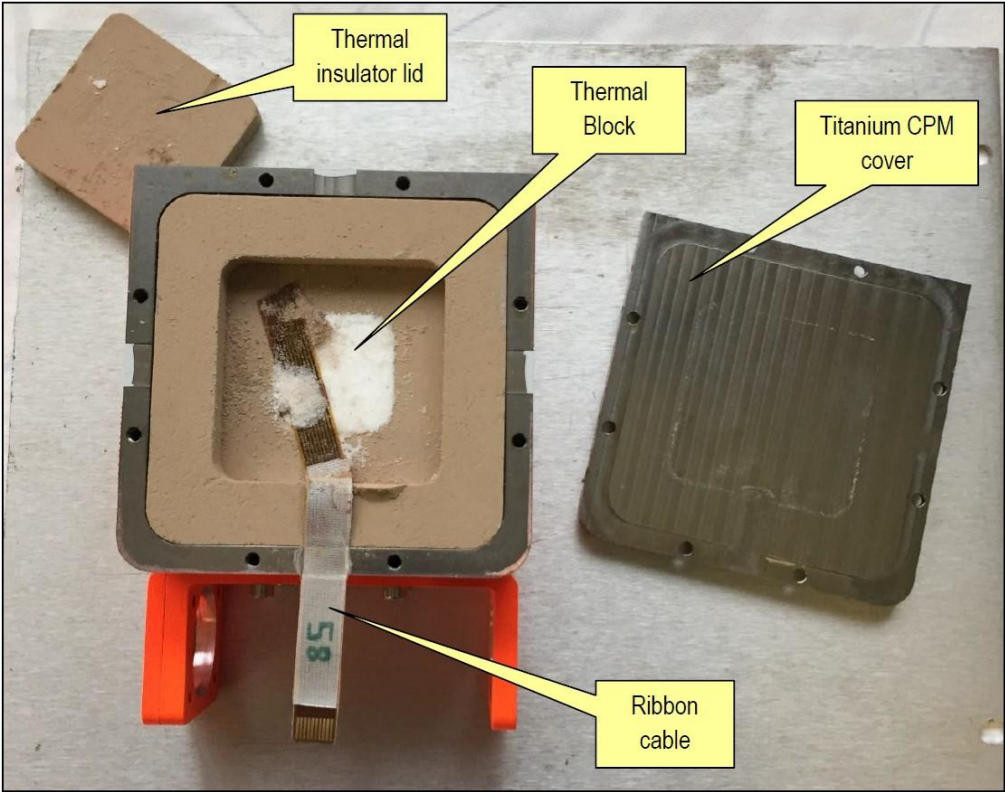
Data extraction via internal SATA

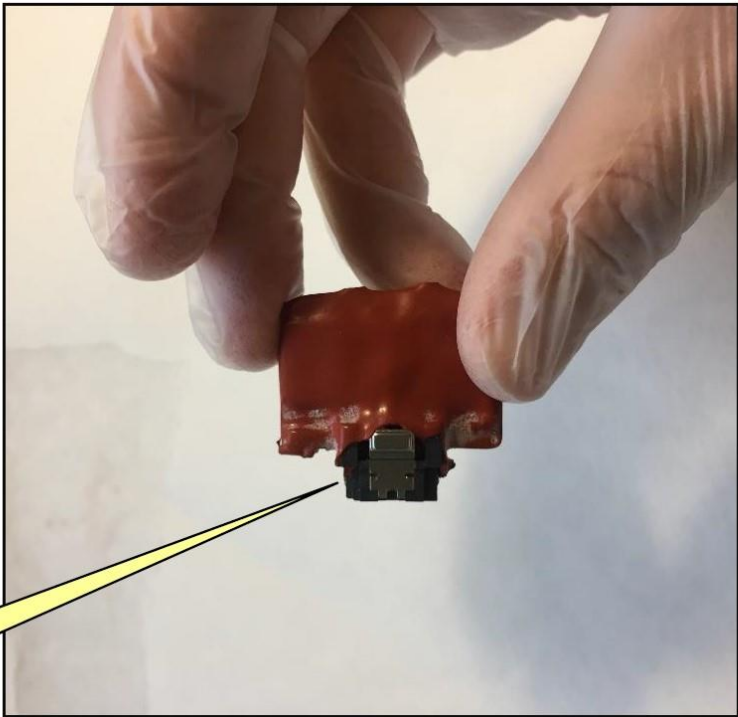
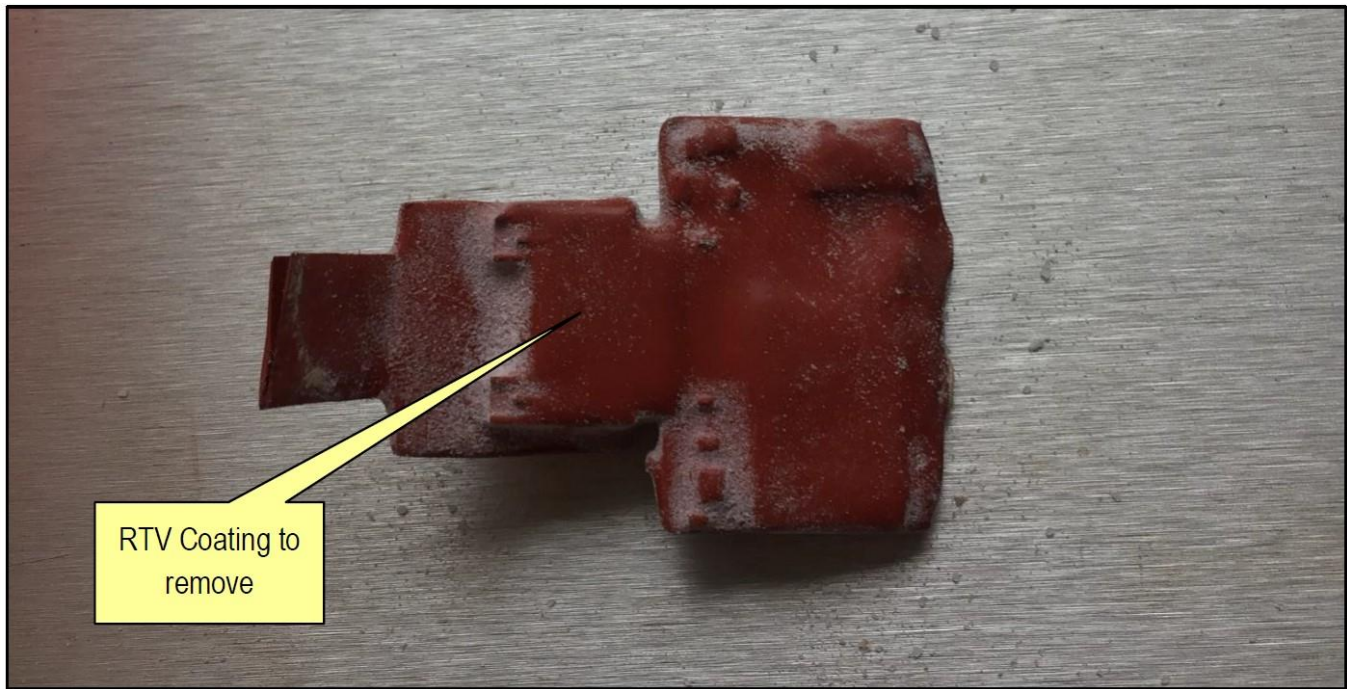


Real-world test...

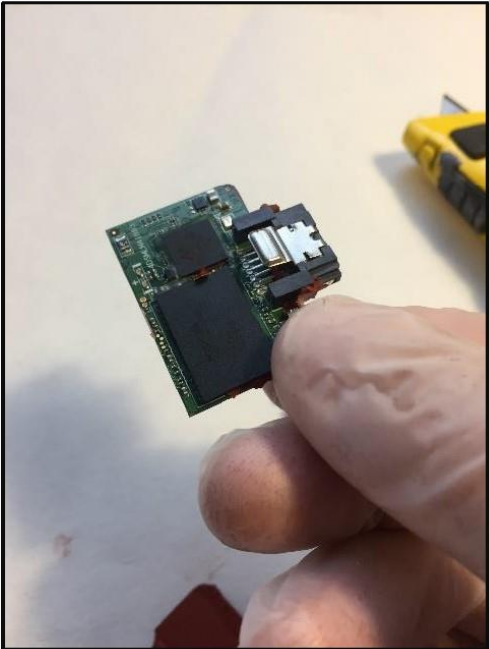
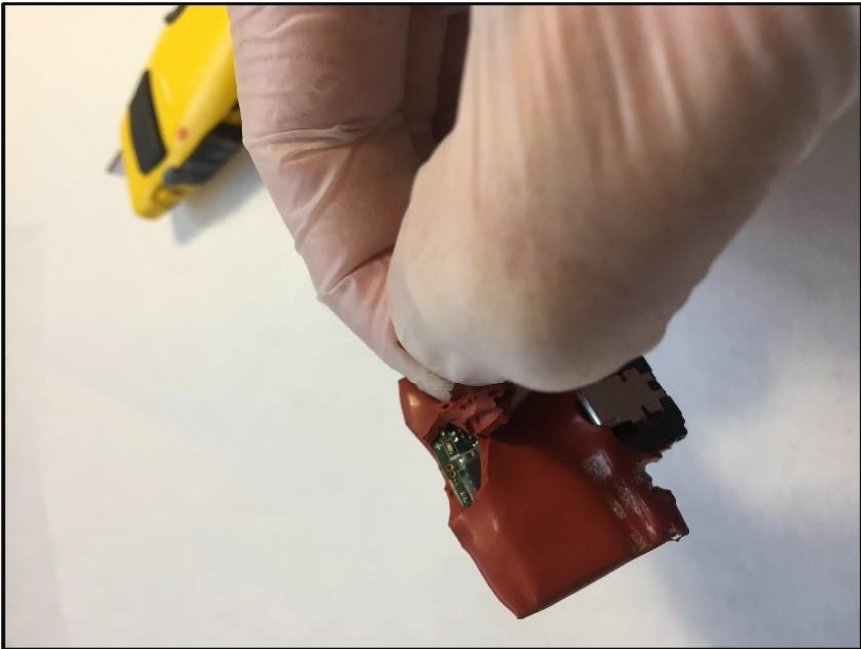


When everything else fails...chips usually don't





FORTUNATELY, real-world crash conditions are rare occasion, we were not able to get our hands on damaged device

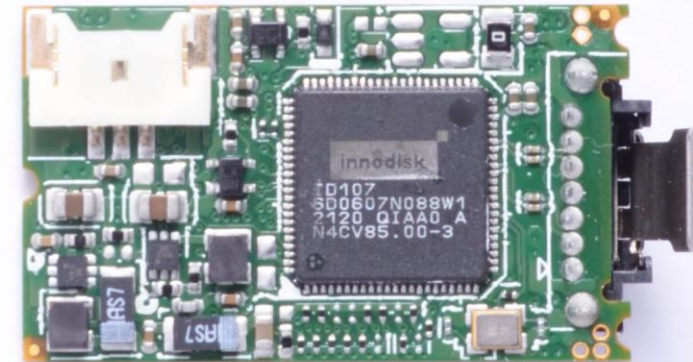




On the other side of PCB we can see the microcontroller

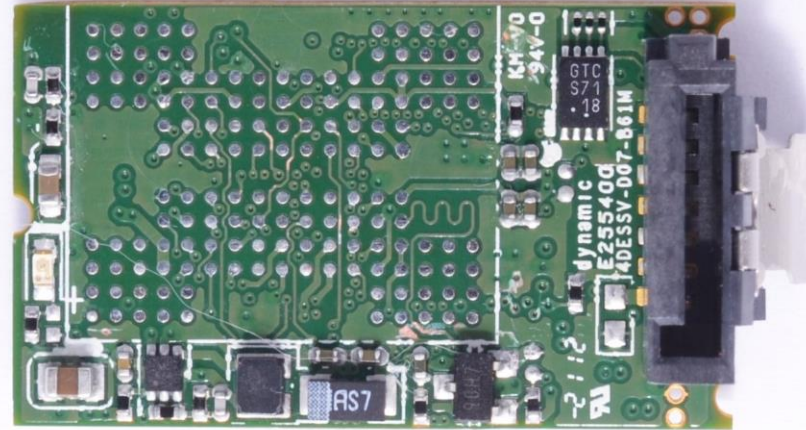


On this side of PCB we can spot NAND memory chip made by Kioxia (Toshiba) with the model name TH58TEG8H2HBA-89

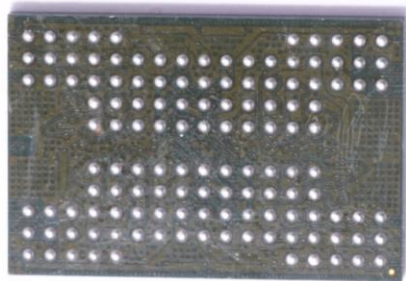
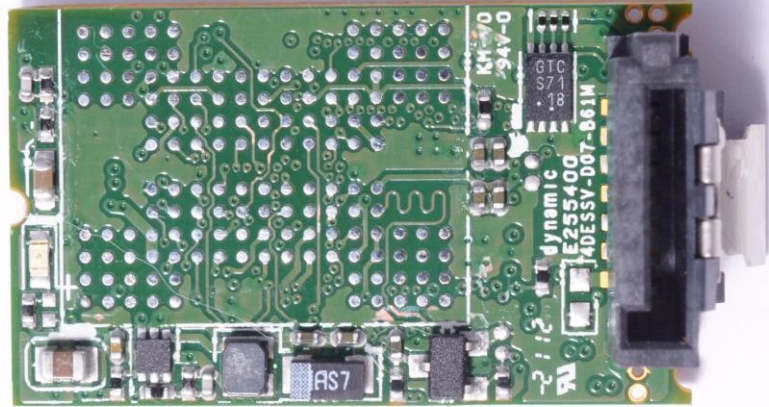


Unsoldered NAND memory – top view

The memory chip was removed from the PCB for further reading using InfraRed rework station and thermal profile of Tmax = 240C (Tdelta ~ 3C/s)



Unsoldered NAND memory – ball view



The NAND memory has BGA-132 package which is classics for high-capacity memory chips. The pads of NAND memory chip have been cleaned with solder wick and then isopropyl alcohol.

Visual NAND Reconstructor

Physical image reconstruction in VNR

The screenshot displays the VNR interface with the following components:

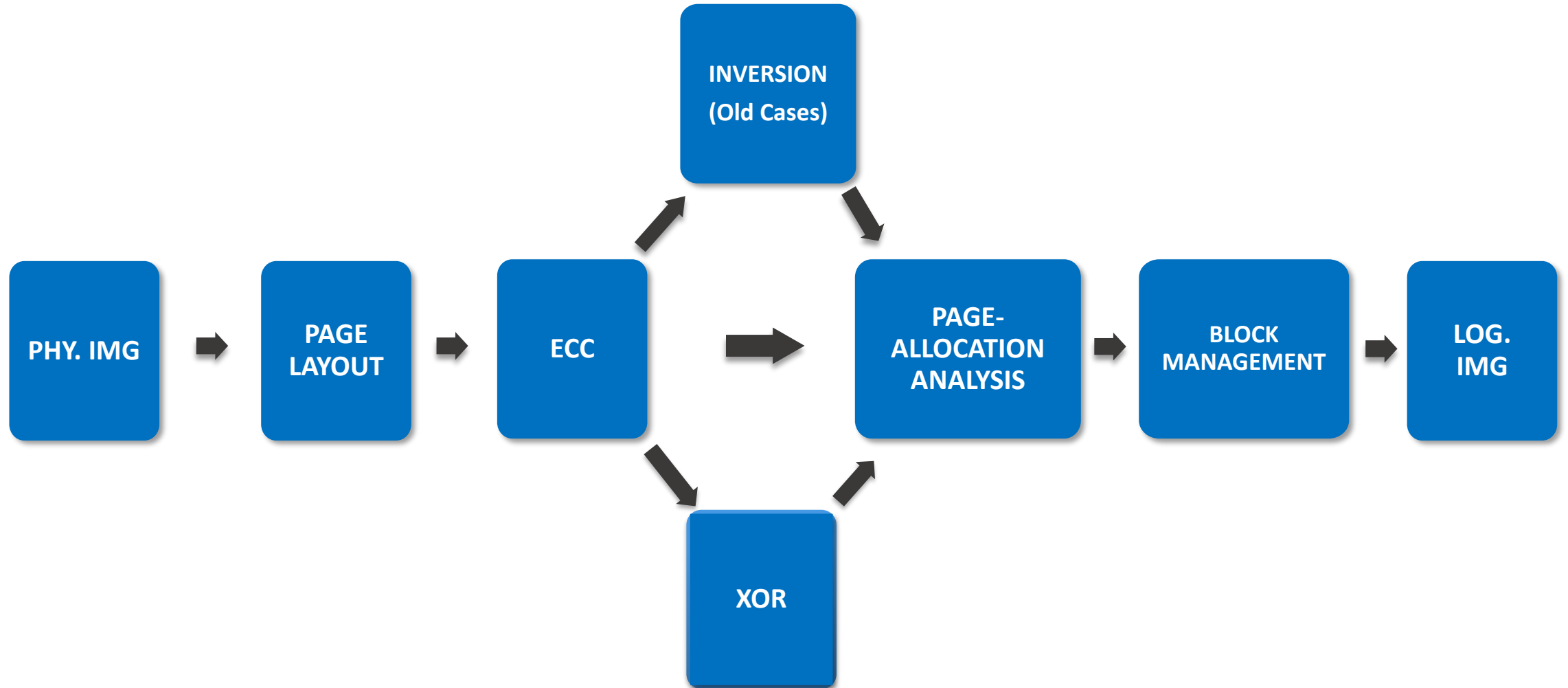
- Case:** Solution type: Controller; Device type: Memory chip ID; Device name: Number of memory chips: 1; Pinout: Number of crystals: 1. Author: Rusolut. Premium Support is active till 07 Mar 2024. [Help center](#)
- Workspace:** Element functions: Delete, Copy, Paste, Open images, Send solution to Db, Insert area, Skip area, Extract area.
- Diagram:** A flowchart showing the reconstruction process: Reader (0) → Phy image (Chip0_0_0) → ECC (0) → XOR (0) → Pair (0) → Markers table (0) → Log image (0).
- Elements Panel:**
 - Dump operations
 - Block list operations
 - Other:
 - R Reader
 - PI Physical image
 - BCR Bad byte col. remover
 - bBCR Bad bit col. remover
 - BCH ECC
 - I Inversion
 - X XOR
 - P Pair
 - U Unite
 - O Offsets
 - LI Logical image

Data extraction

The screenshot displays the VNR interface with the following components:

- Case:** File system viewer. Check headers, Save image, Save selected, Check file system, Create unallocated data dump, Correct allocated, Correct unallocated, Correct selected files data, Android data extractor, SQLite carver, Refresh.
- Workspace:** Log image 0 X. Workspace. GPT ▶ Volume5 (EXT-family) /data 2.08 GB ▶ Root ▶
- File System View:**
 - Dump
 - MBR
 - GPT
 - Volume0 (EXT-family) 16.00 MB
 - Volume1 (Microsoft FAT16) NO NAME 64.00 MB
 - Volume2 (EXT-family) /persist 4.00 MB
 - Volume3 (EXT-family) /system 1.17 GB
 - Volume4 (EXT-family) 250.00 MB
 - Volume5 (EXT-family) /data 2.08 GB
 - Root
 - app
 - app-asec
 - app-private
 - audio
 - backup
 - bms
 - controlcenter
 - dalvik-cache
 - data
 - dontpanic
 - drm
 - efslog
 - etc
 - fota
 - hdcp
 - last_alog
 - last_kmsg
 - local
 - lost+found
 - media
 - mediaserver
 - misc
 - property
 - resource-cache
 - shared
 - smime
 - ssh
 - startupservice
 - suntory

Chip-off data recovery procedure



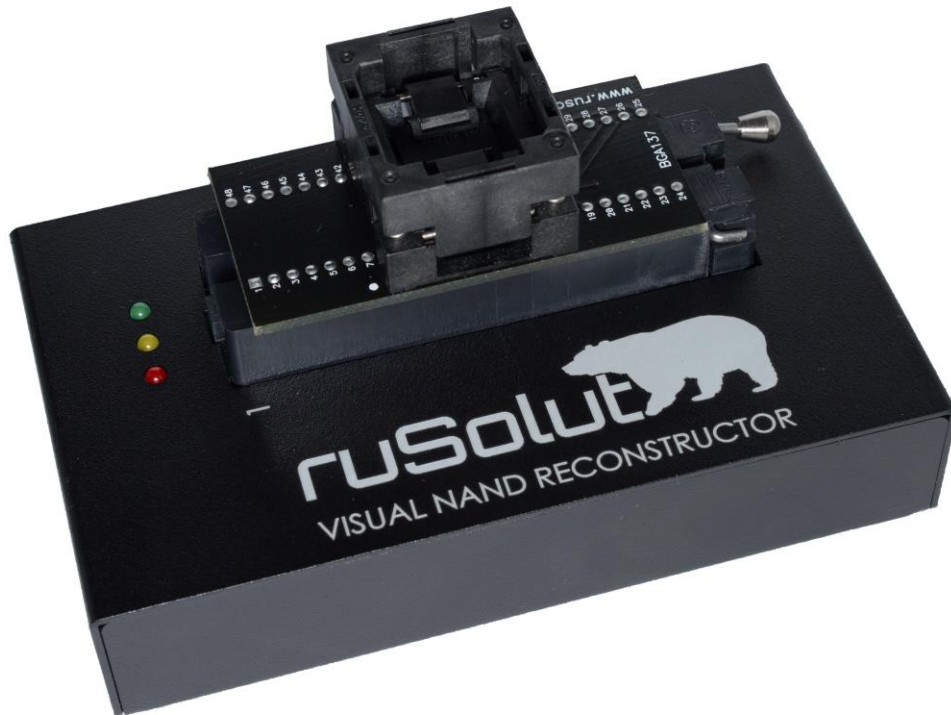
Chip connected to VNR Reader

We used Visual Nand Reconstructor Reader from Starter kit in couple with BGA132 adapter from Standard kit for memory chip reading.

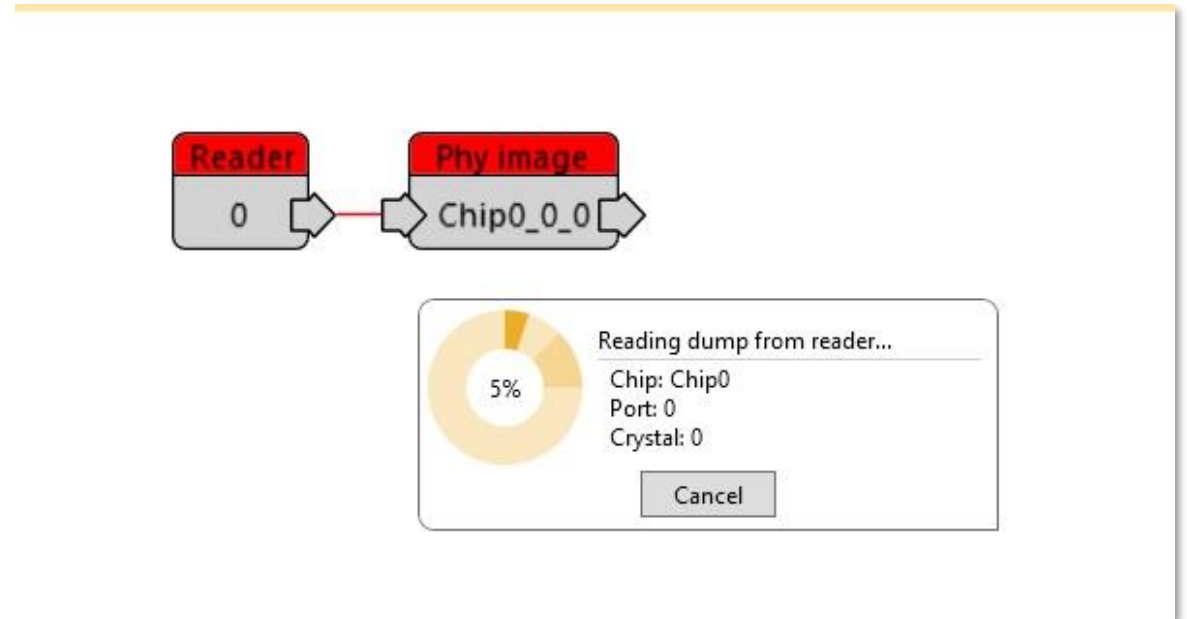


Physical image extraction

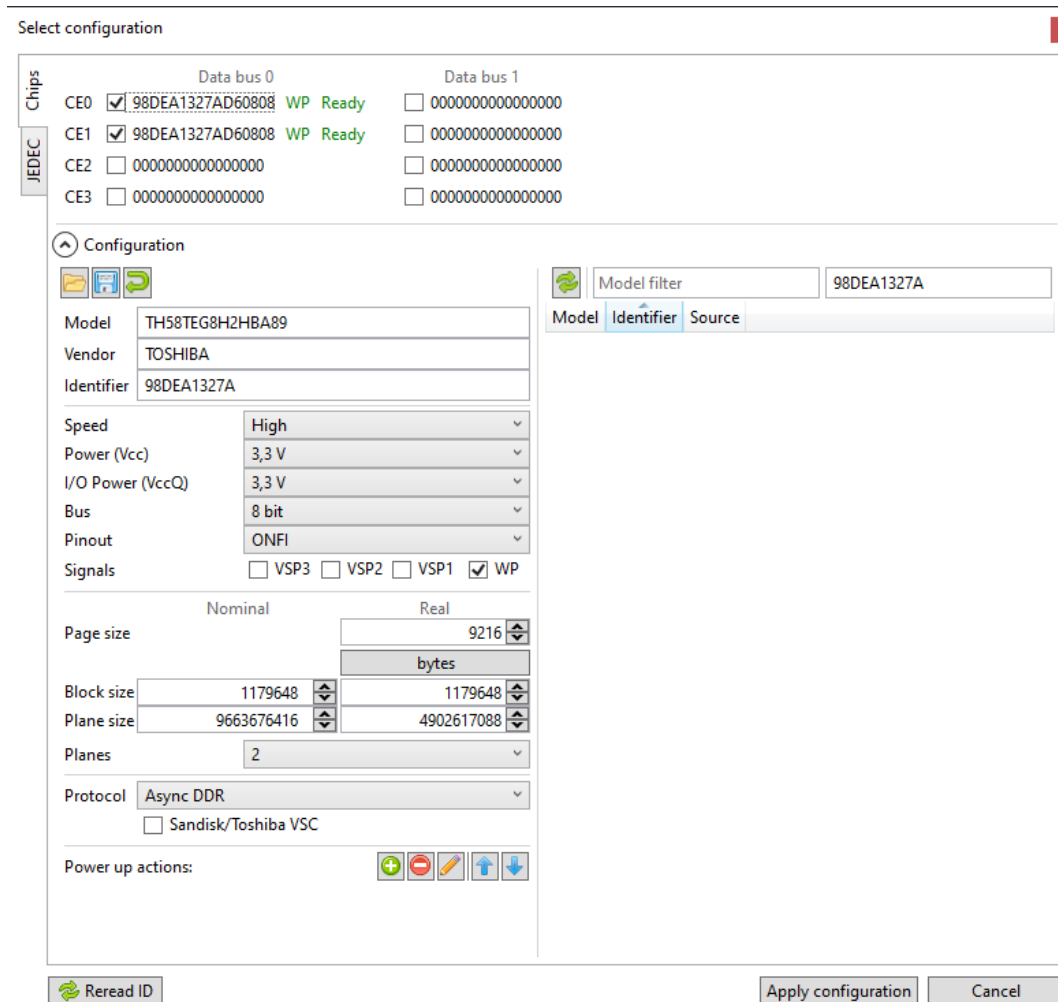
Device in the VNR Reader



Reading initialised in the software



Memory chip identification



The first step before physical image reading is reading memory chip's ID.

The chip model identifier is 98DEA1327A which belongs to Toshiba/Kioxia manufacturer

The memory chip has multi-die structure and we were able to identify 4 dies/crystals in single package.

JEDEC data

Select configuration

Chips	JEDEC
Parameter page signature	JESD
Revision number	supports vendor specific parameter page
Features supported	no
Optional commands supported	no
Secondary commands supported	no
Number of parameter pages	0x0
Device manufacturer	TOSHIBA
Device model	TH58TEG8H2HBA89
JEDEC manufacturer ID	00000000098
Number of data bytes per page	0x2000
Number of spare bytes per page	0x400
Number of pages per block	0x80
Number of blocks per logical unit (LUN)	0x103C
Number of logical units (LUNs)	0x2
Number of Address Cycles	row 0x3, column 0x2
Number of bits per cell	0x1
Number of programs per page	0x0
Multi-plane addressing	0x1 bits for plane address
Multi-plane operation attributes	no
Asynchronous SDR speed grade	no
Toggle Mode DDR and NV-DDR2 speed grade	supports 30 ns speed grade (~33 MHz) supports 25 ns speed grade (40 MHz) supports 15 ns speed grade (~66 MHz) supports 12 ns speed grade (~83 MHz) supports 10 ns speed grade (100 MHz) supports 7.5 ns speed grade (~133 MHz) supports 6 ns speed grade (~166 MHz) supports 5 ns speed grade (200 MHz)
Synchronous DDR speed grade	no
Asynchronous SDR features	0x0
Toggle-mode DDR features	0x0
Synchronous DDR features	no
Maximum page program time (tPROG)	0 us
Maximum block erase time (tBERS)	0 us

Apply configuration

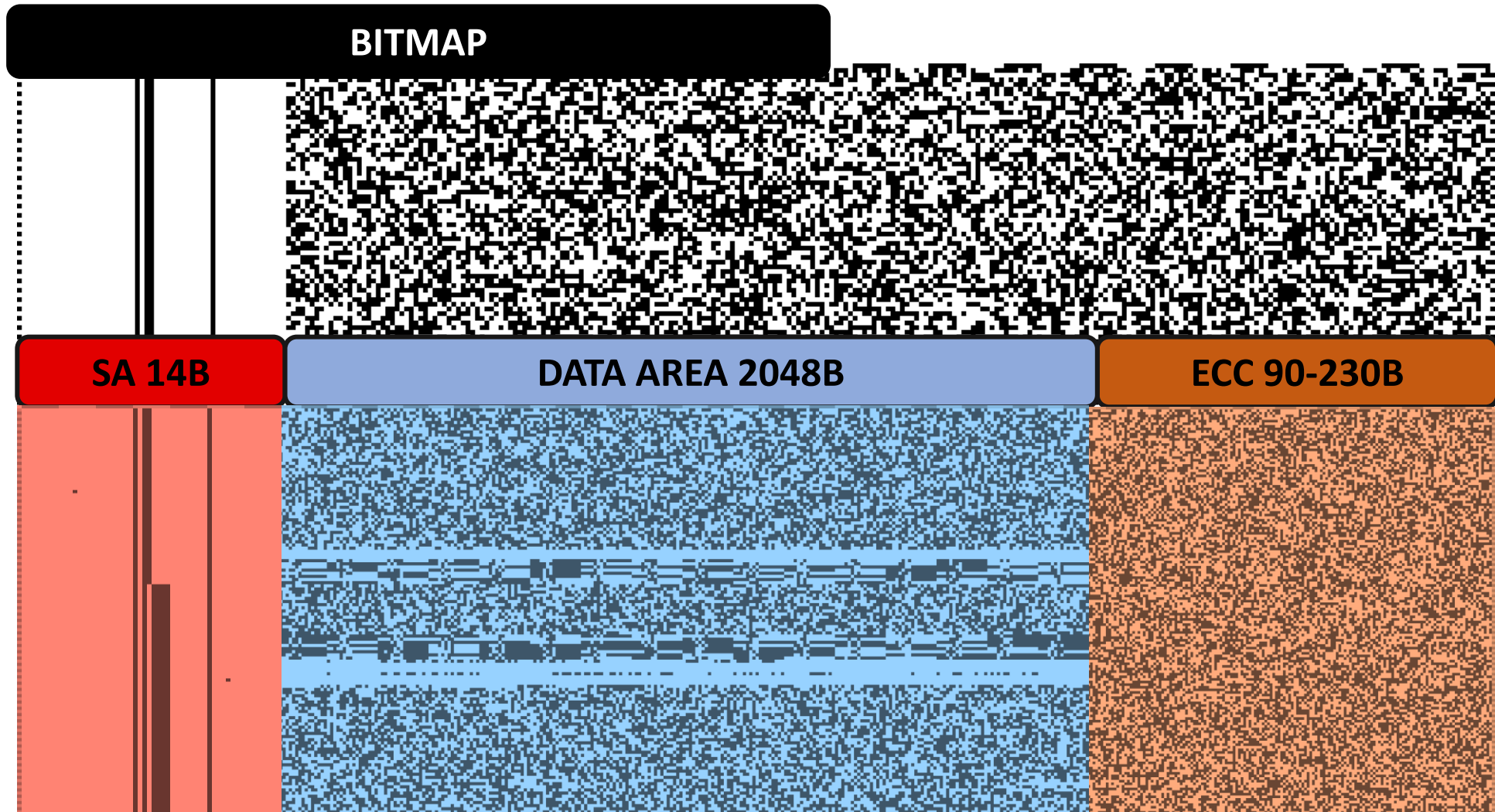
Reread ID

Apply configuration Cancel

This NAND chip has special JEDEC parameter page that shows basic information about the memory.

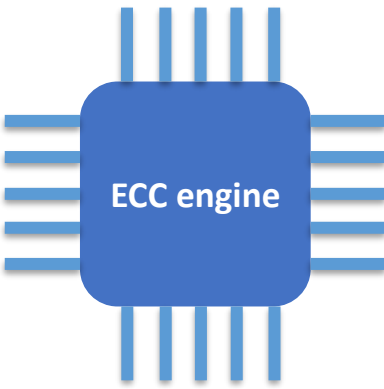
As we can see from report:
Number of bits per cell = 1,
which means that memory chip has **SLC architecture, and it is the best choice for the applications where reliability is a KEY factor.**

Page layout



Error Correction Code(ECC)

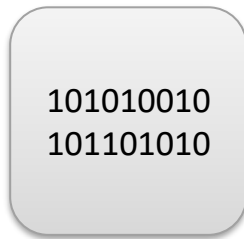
Scrambled data
1024 bytes



Scrambled data
1024 bytes



ECC
10-250 bytes



ECC
algorithms

Hamming code (OLD)

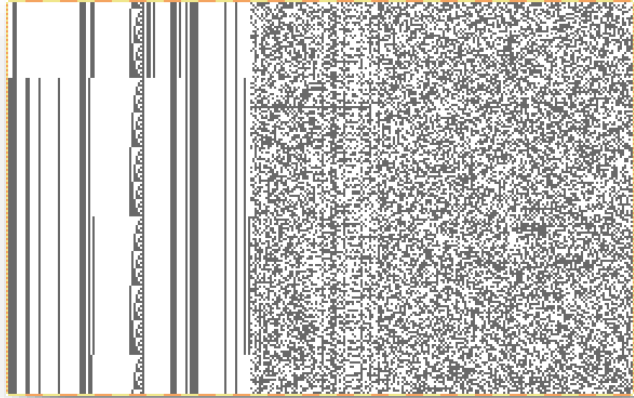
Reed-Solomon code (OLD)

BCH

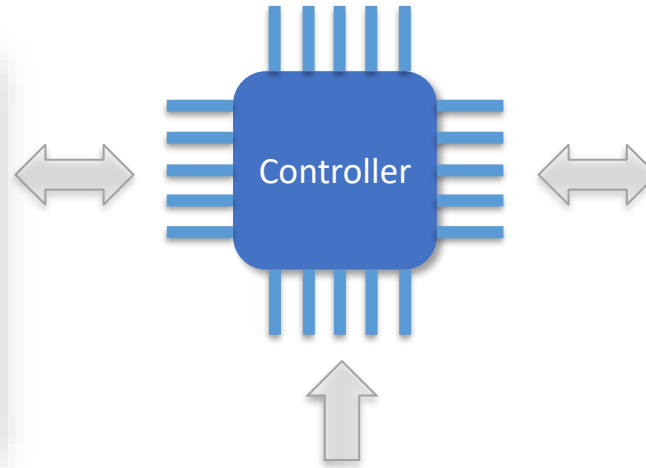
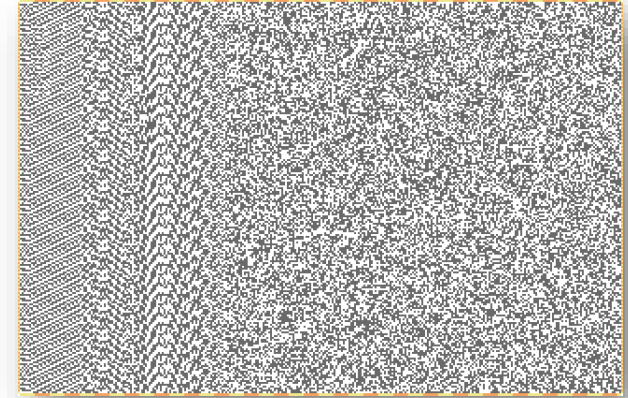
LDPC

Scrambler XOR key

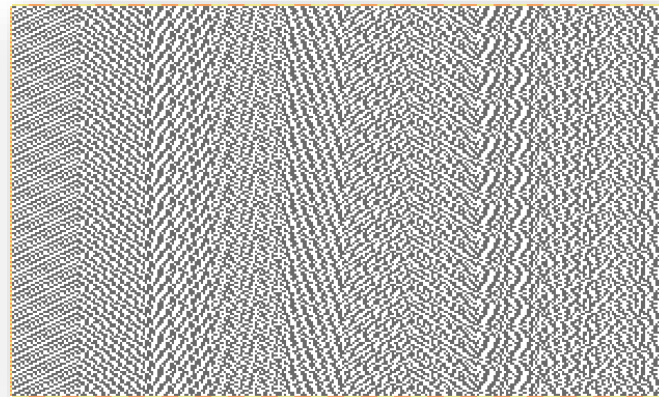
DATA



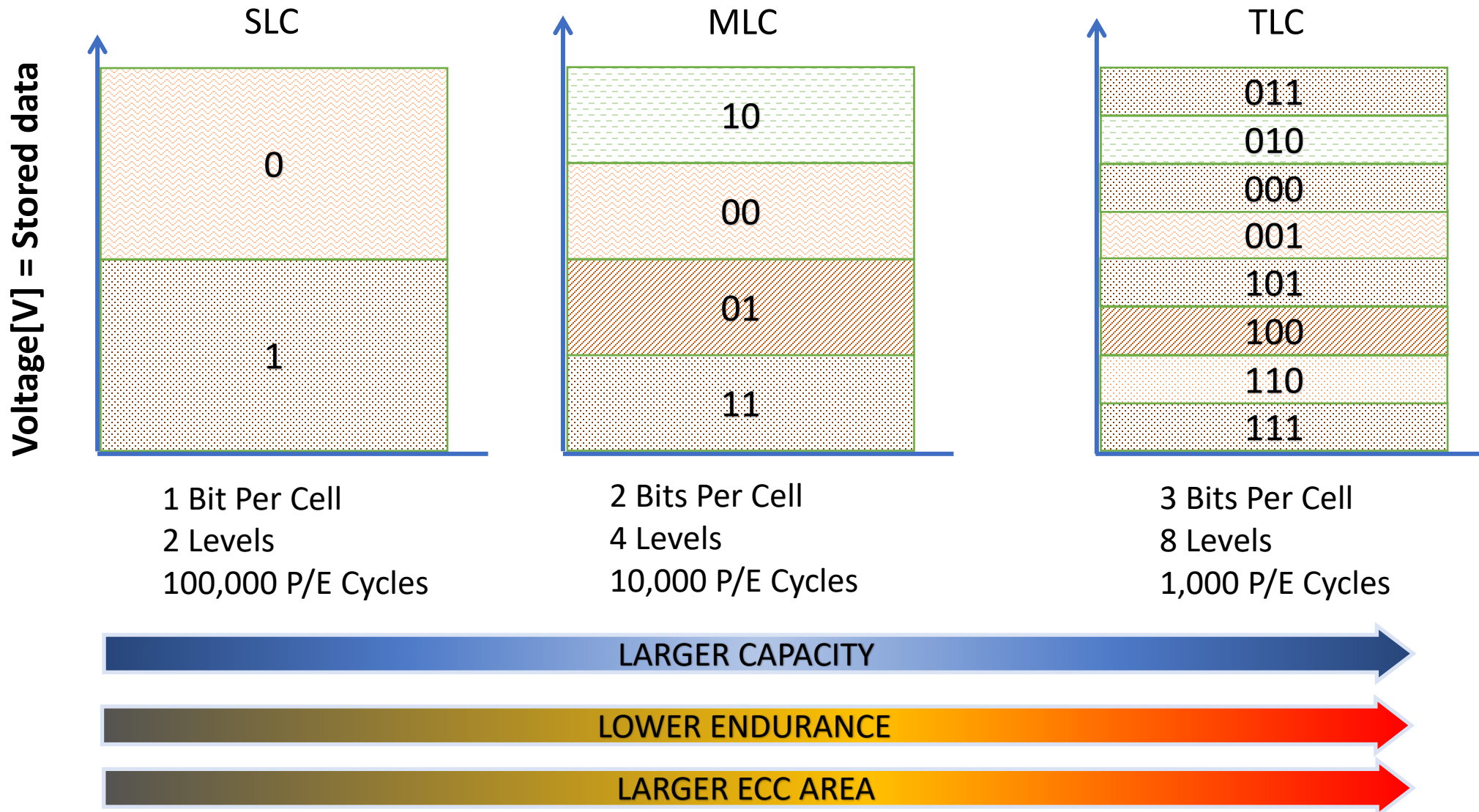
SCRAMBLED DATA



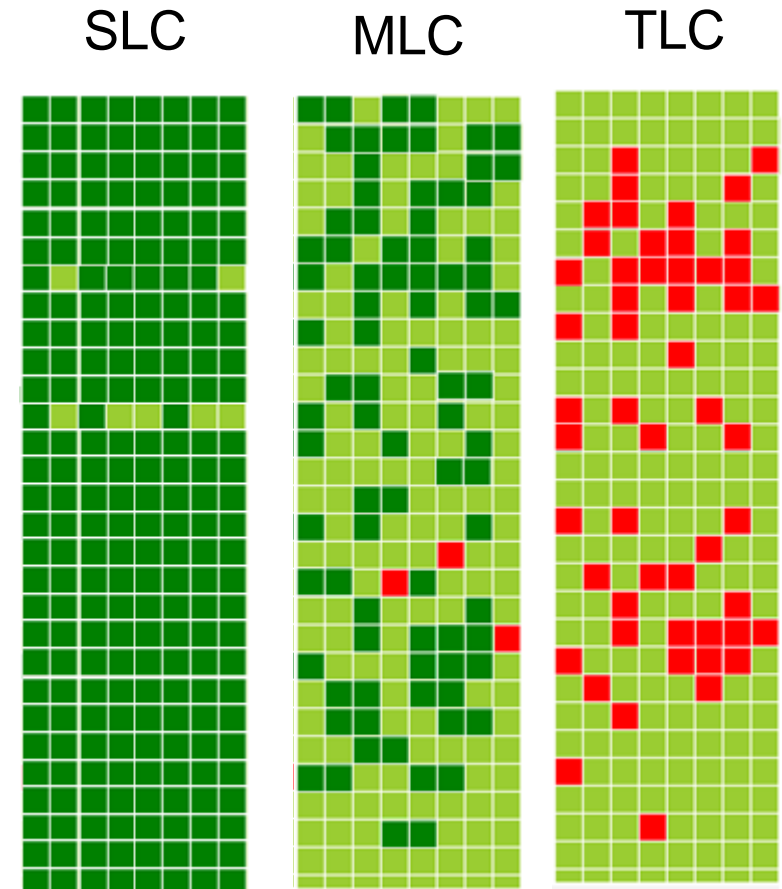
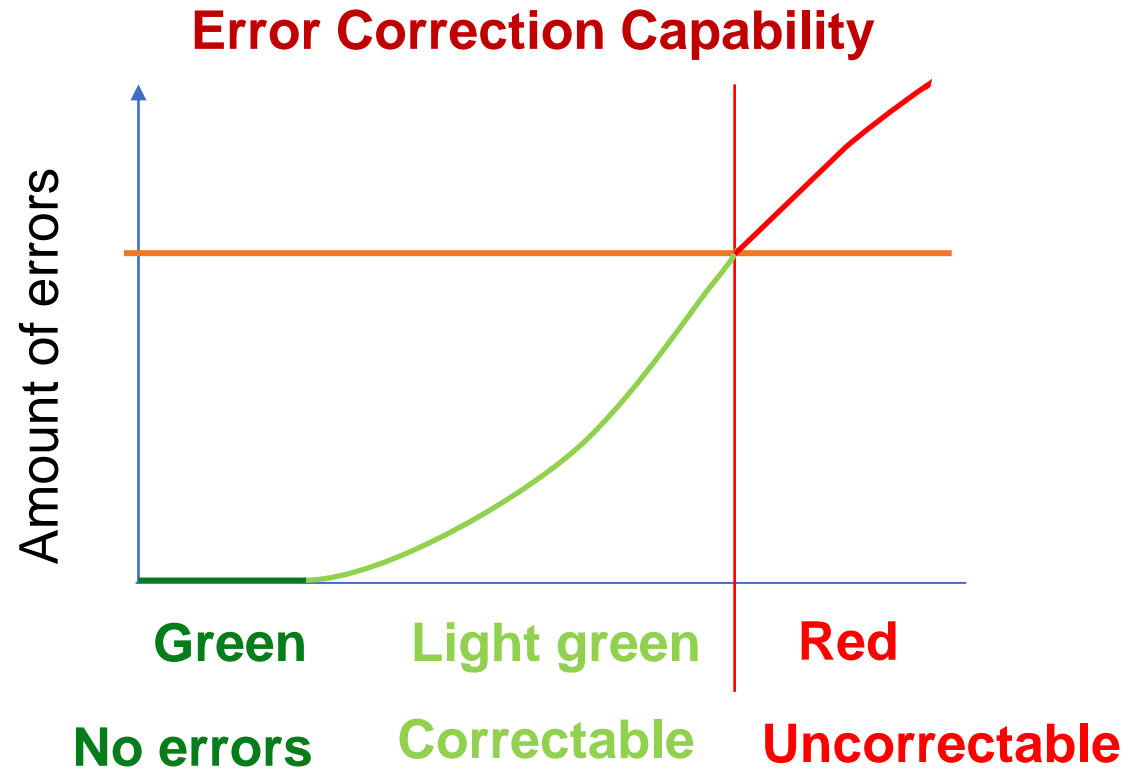
XOR key



NAND memory cell architectures

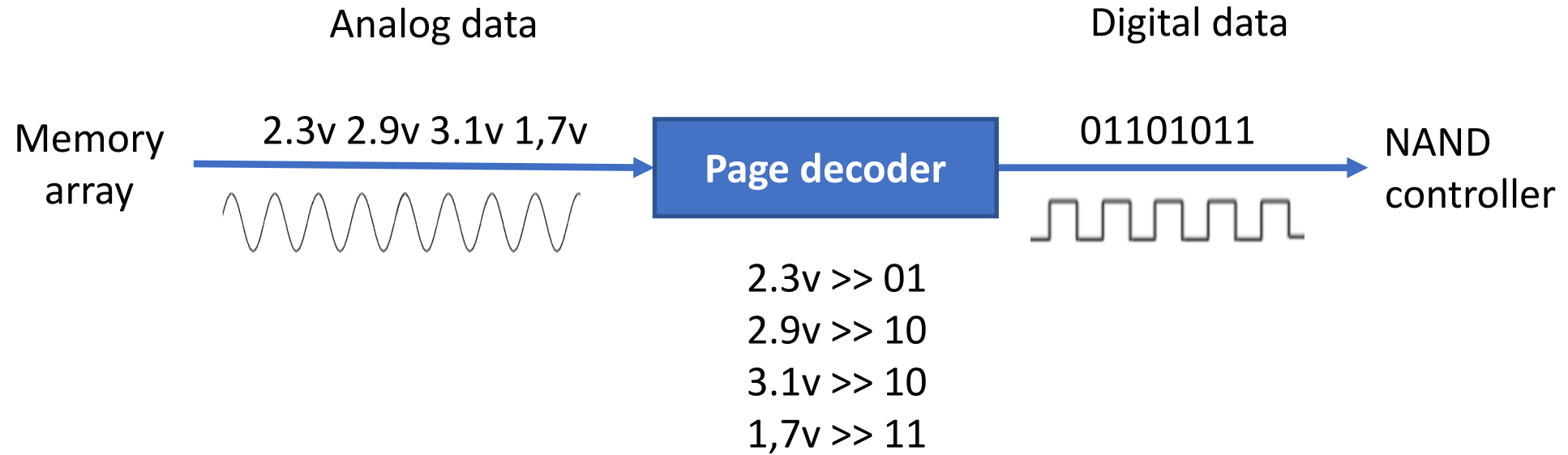


Bit errors in NAND



Page decoder

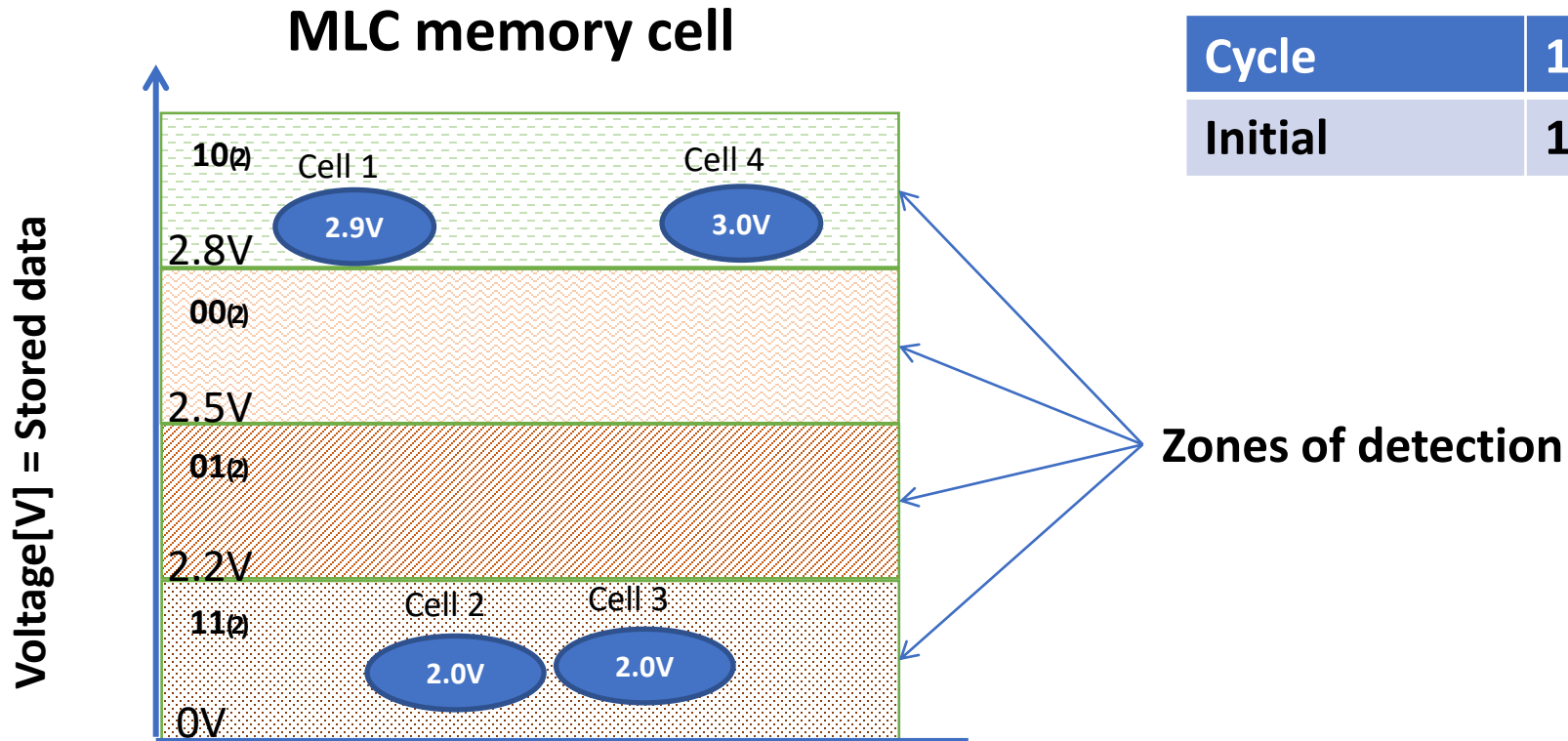
Analog states from cells are converted into digital data



Bits inside memory cell

The data in cell is stored as a voltage level

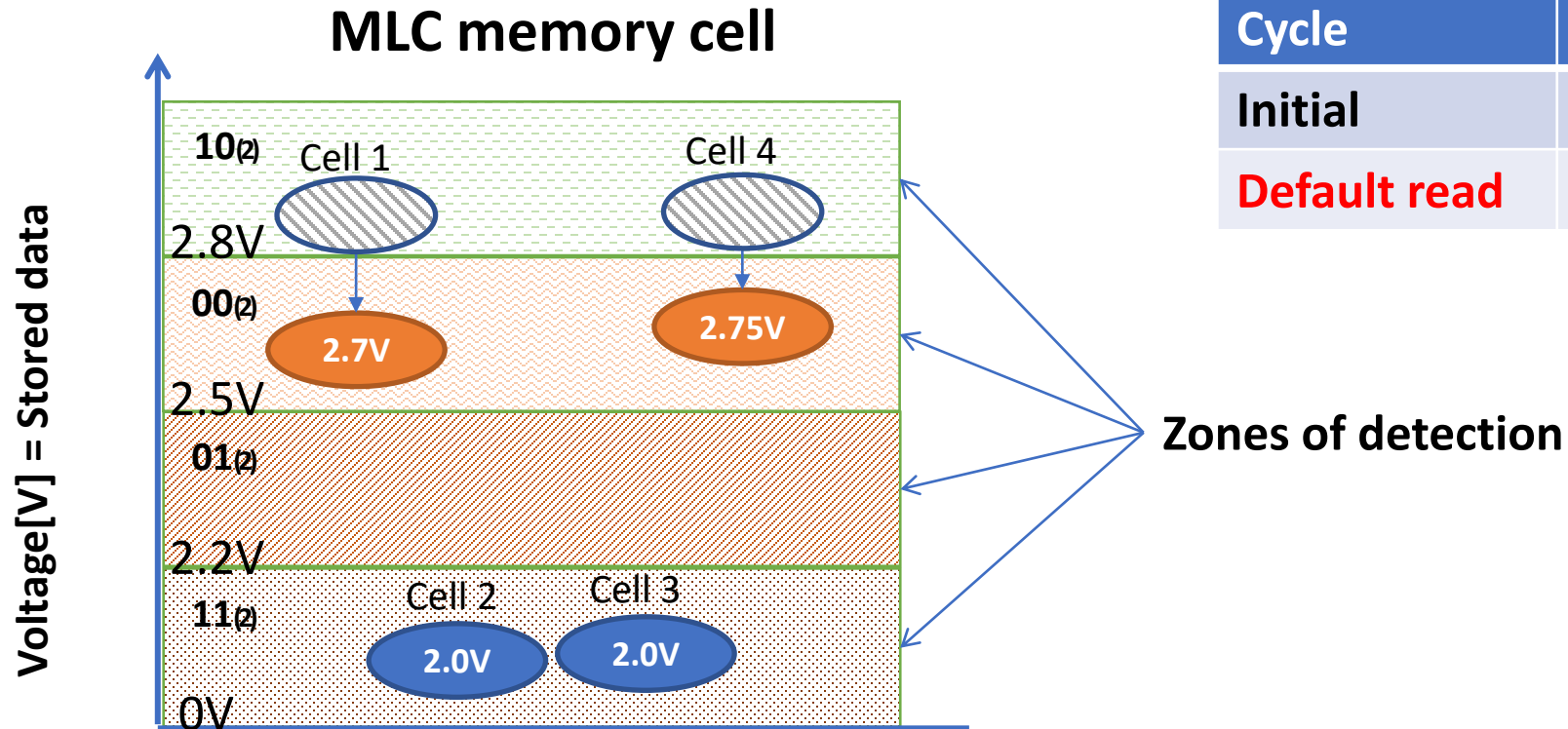
Controller is reading data according to specific zones



Cycle	1	2	3	4	HEX
Initial	10	11	11	10	BE

Retention Error

When charge leaks out from cell we get bit error

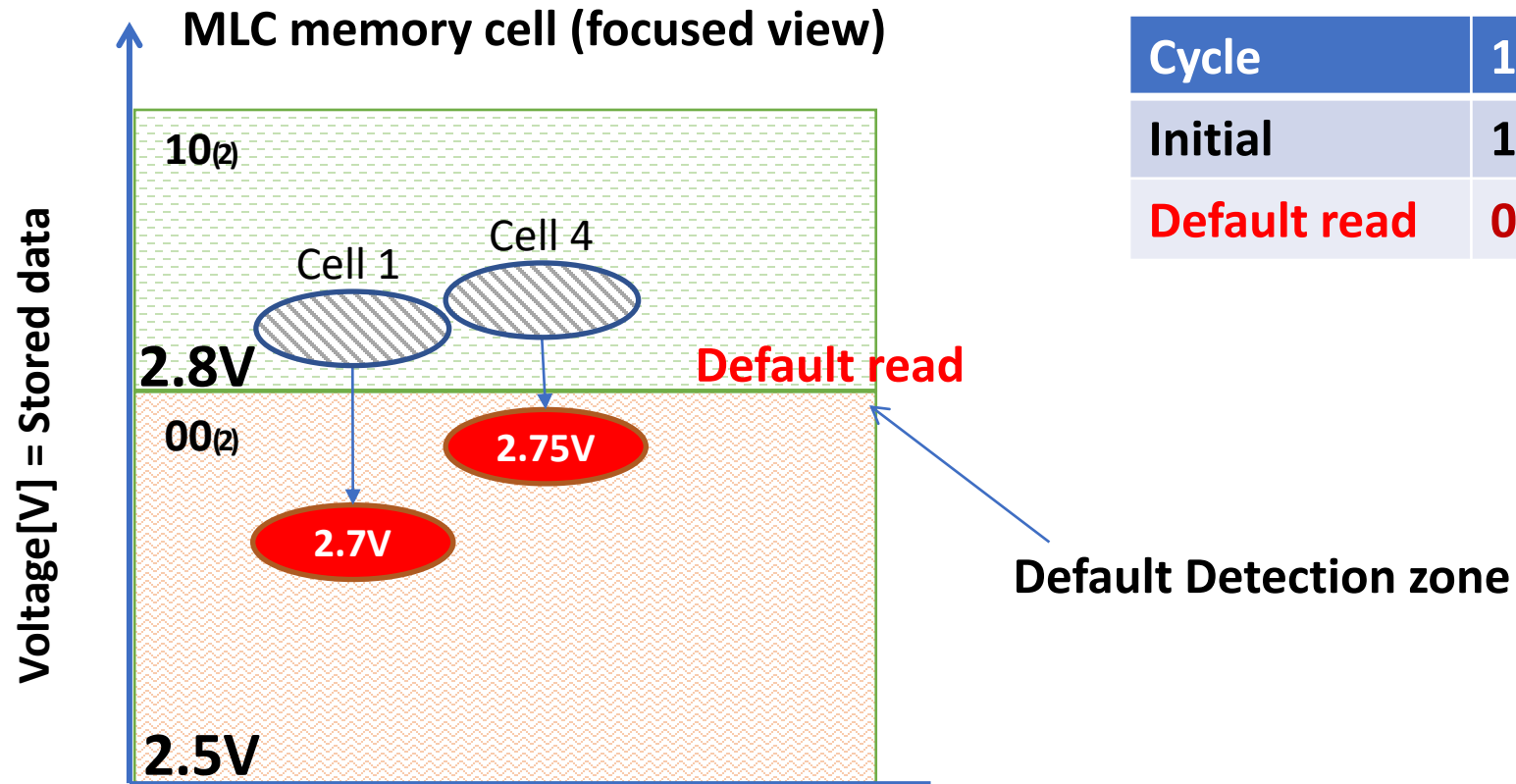


Cycle	1	2	3	4	HEX
Initial	10	11	11	10	BE
Default read	00	11	11	00	3C

Read-Retry Mechanism

When charge leaks out from cell we get bit error

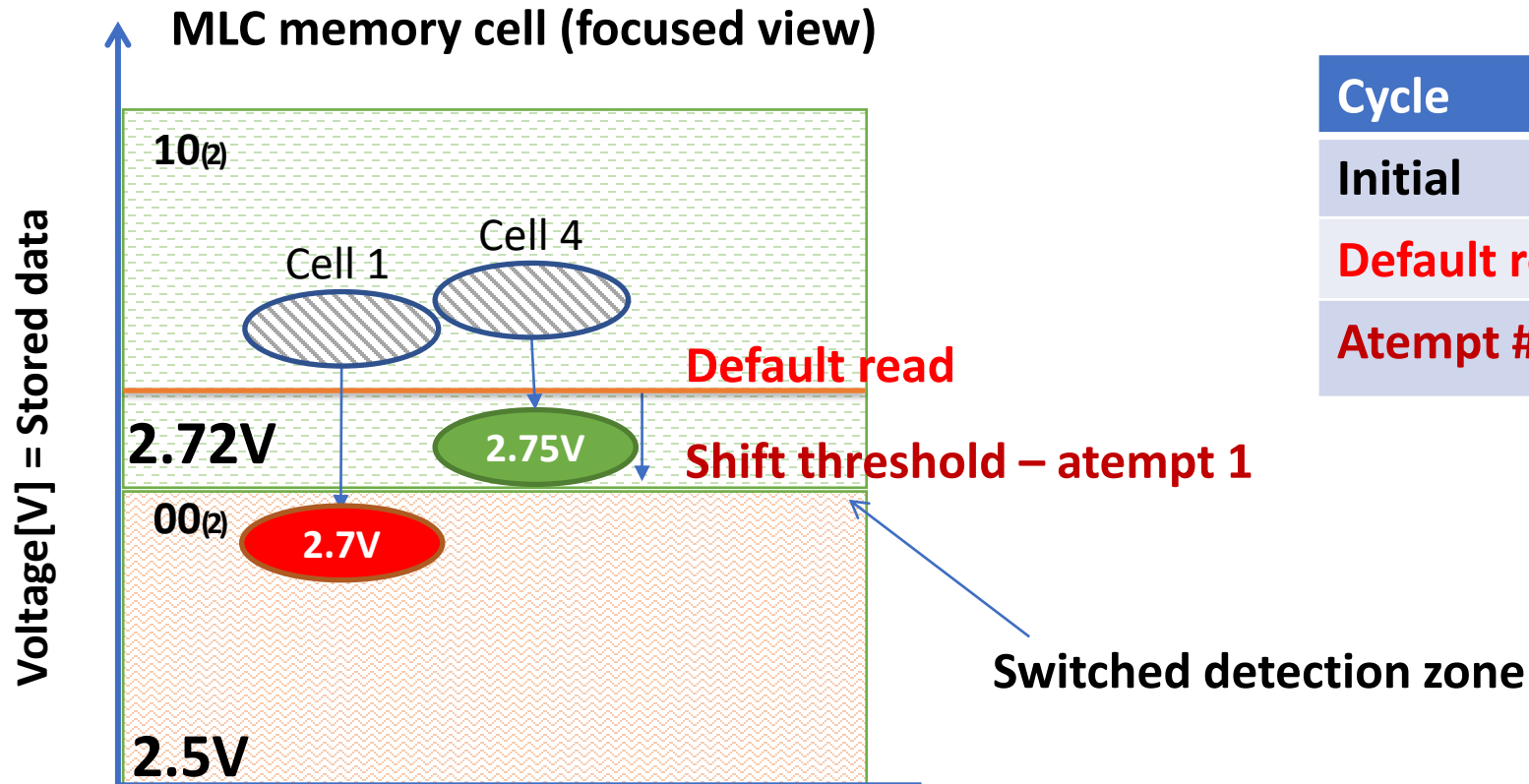
Degraded cell gives wrong data



Cycle	1	2	3	4	HEX
Initial	10	11	11	10	BE
Default read	00	11	11	00	3C

Read-Retry Mechanism #1

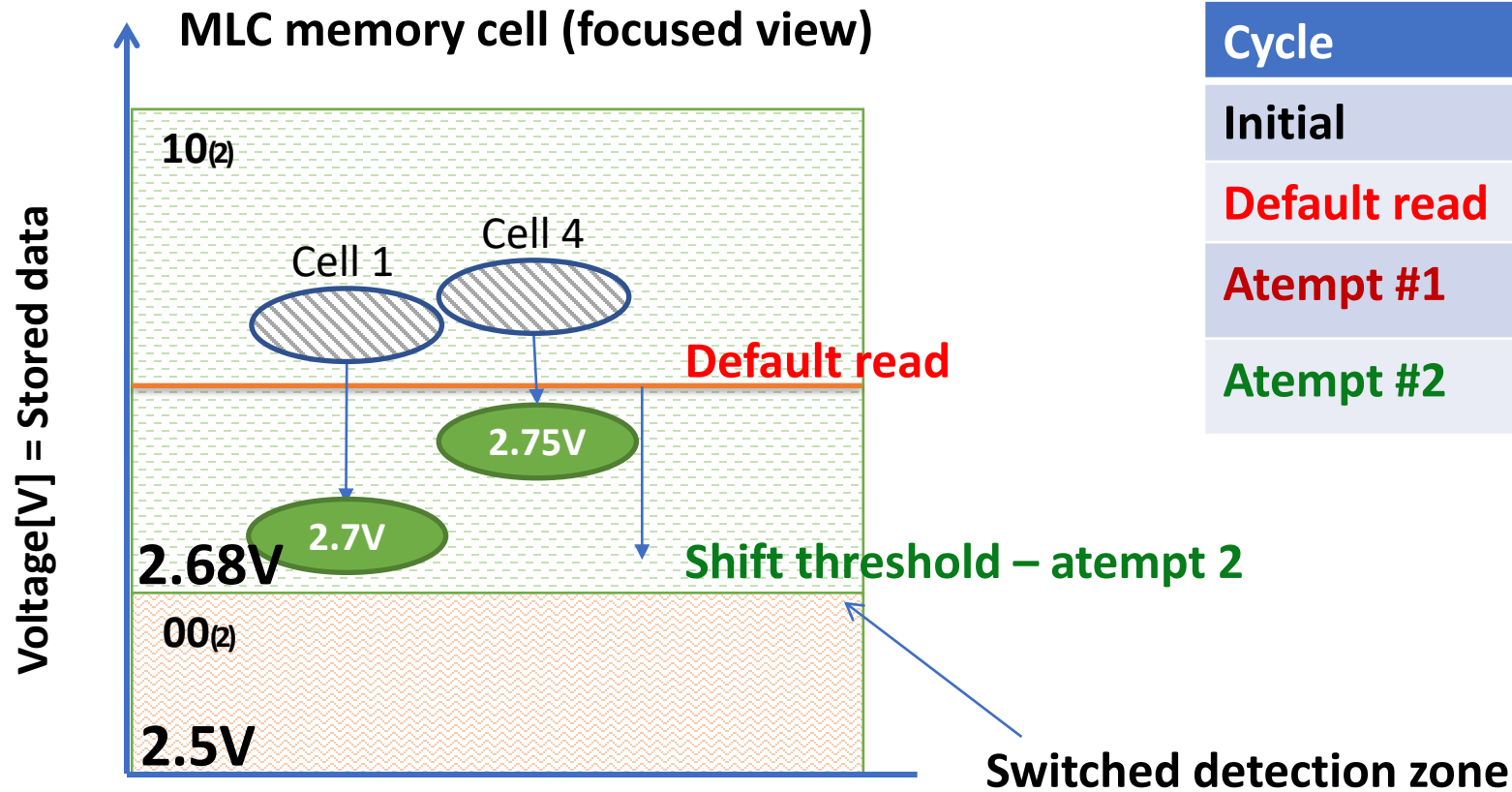
Read retry mechanism helps to shift read voltage thresholds



Cycle	1	2	3	4	HEX
Initial	10	11	11	10	BE
Default read	00	11	11	00	3C
Attempt #1	00	11	11	10	3E

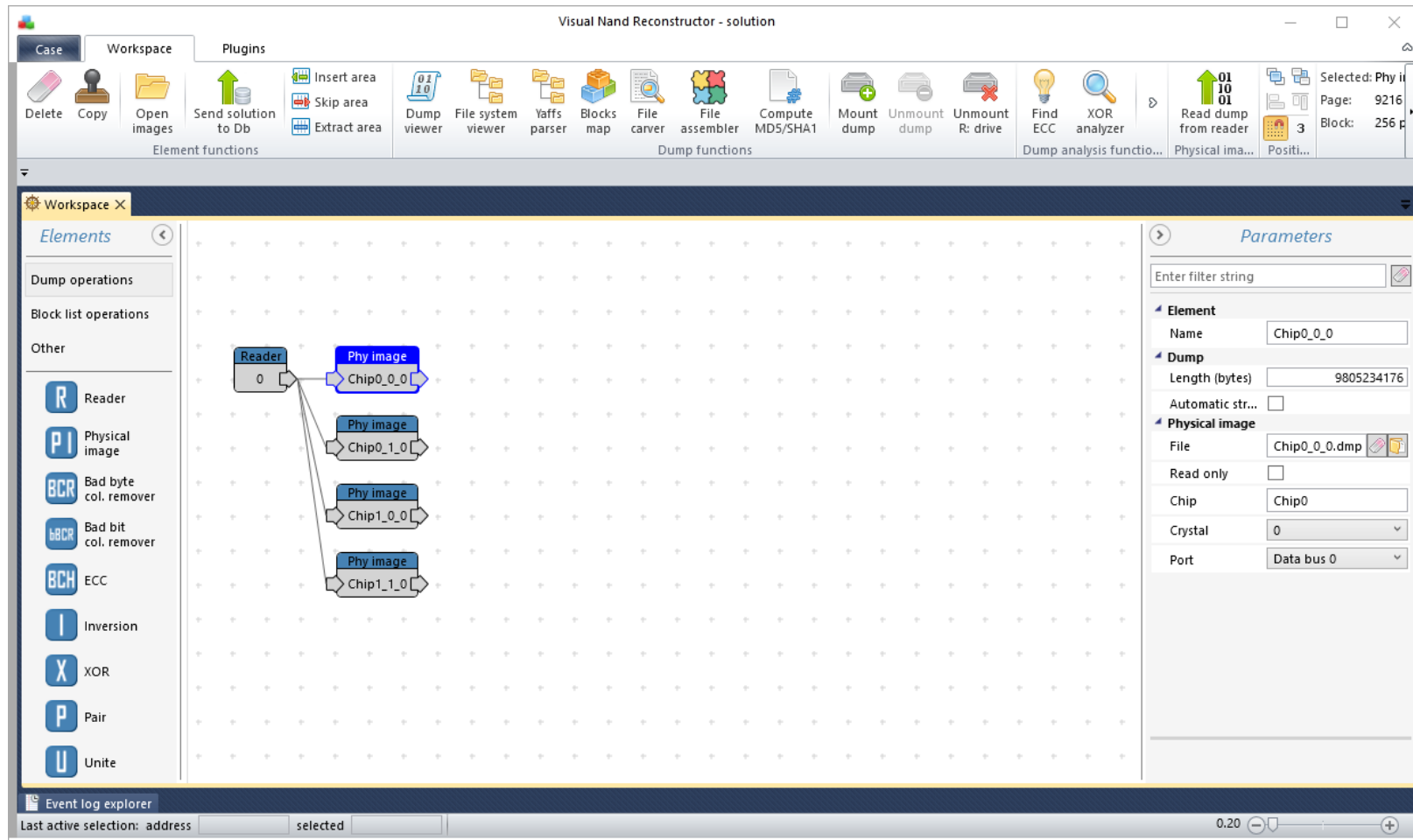
Read-Retry Mechanism #2

Read retry mechanism helps to shift read voltage thresholds



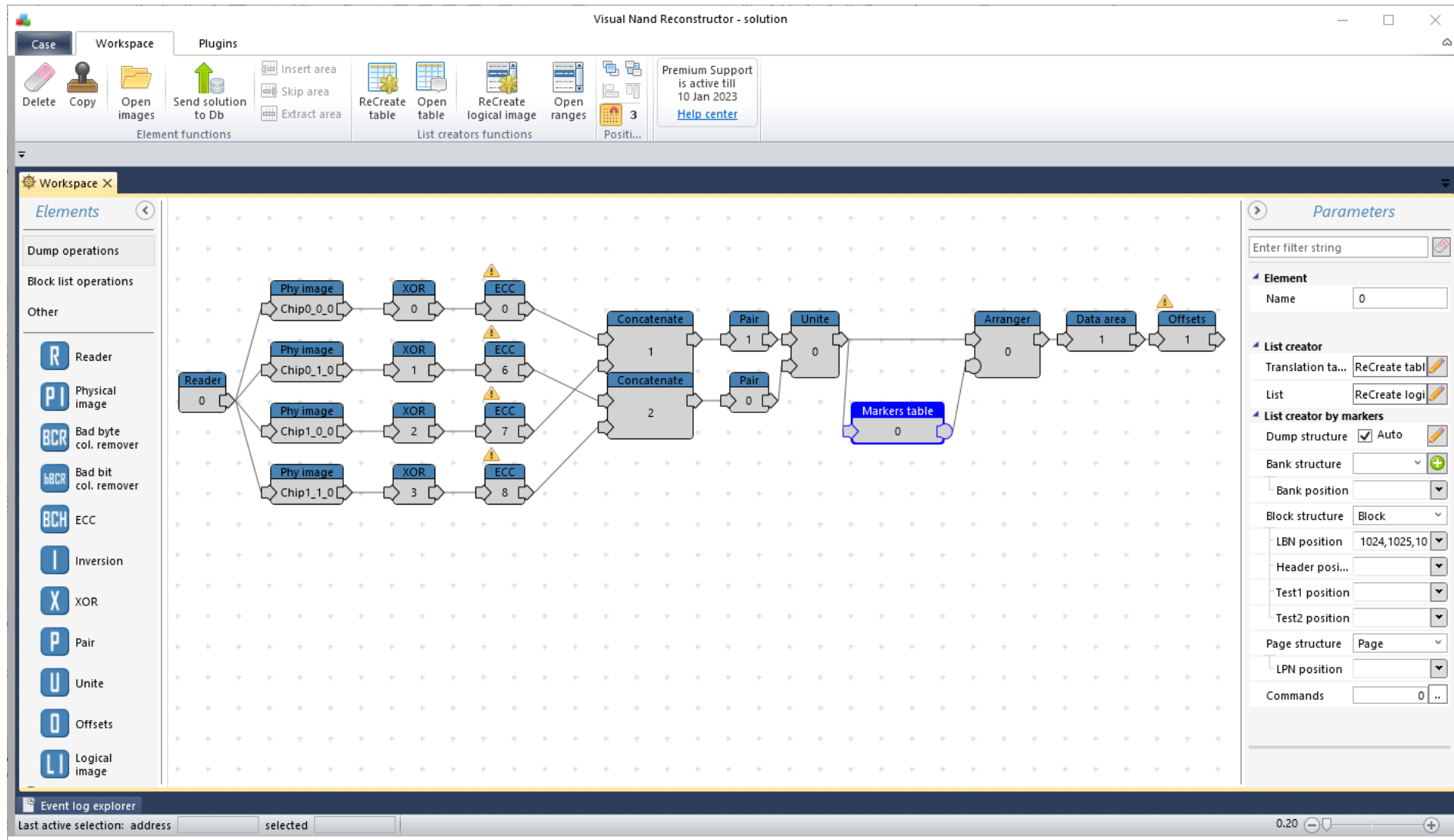
Cycle	1	2	3	4	HEX
Initial	10	11	11	10	BE
Default read	00	11	11	00	3C
Attempt #1	00	11	11	10	3E
Attempt #2	10	11	11	10	BE

Physical image extraction from NAND



We used Visual NAND Reconstructor for memory chip reading and physical image processing. In total 4 dumps/physical images were extracted out of the NAND.

Reconstruction of controller's workflow



Physical image has been converted to logical image through controller's emulation process

ECC algorithm for bit error correction has been found and errors got corrected

The screenshot displays the Visual NAND Reconstructor interface. The main workspace shows a workflow diagram starting with a 'Reader' element (0) that feeds into four 'Phy image' elements (Chip0_0_0, Chip0_1_0, Chip1_0_0, Chip1_1_0). Each phy image is processed by an 'XOR' element (0-3) and then an 'ECC' element (0-8). The ECC elements are connected to two 'Concatenate' elements (1 and 2), which are then processed by 'Pair' elements (1 and 0). The 'Parameters' panel on the right shows the 'ECC corrector' settings, including 'Power' set to 'Off', 'ECC codewords' set to 'JMicron(JM)UMF668_8832(ecc70b)_8.bch', 'Page size' set to 9216, and 'ECC map' checked. Below the parameters is an 'ECC map' grid showing a large area of green cells, indicating that all errors were correctable. The status bar at the bottom shows 'Last active selection: address selected' and a zoom level of 0.20.

Block translation

The screenshot displays the Visual NAND Reconstructor interface. The top toolbar includes options for Markers edit, Block filter, and Block sorter. The main workspace is divided into two panels: 'Block markers' on the left and 'Page markers' on the right. The 'Block markers' table lists physical blocks with columns for Use, Bank, LBN, Address, PBN, LB, and RB. The 'Page markers' table lists logical pages with columns for LPN and Address. The LBN 006D00 is highlighted in blue, corresponding to LPN 00000000. The status bar at the bottom shows 'Position 0x7B from 0x103B' and 'Position 0x0 from 0x3FF'.

Use	Bank	LBN	Address	PBN	LB	RB
<input checked="" type="checkbox"/>	00	006800	0759900000	D11	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006900	08EAA00000	FDA	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006A00	05E7700000	A7F	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006B00	06F0F00000	C57	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006C00	0210C00000	3AC	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006D00	035B800000	5F8	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006E00	072B700000	CBF	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	006F04	004E300000	8B	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007000	02B6200000	4D2	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007100	04F5000000	8D0	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007200	0690C00000	BAC	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007300	07ABB00000	DA3	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007400	0586B00000	9D3	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007500	0907500000	100D	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007600	03ABF00000	687	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007700	03DE900000	6E1	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007800	0106200000	1D2	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007900	0765F00000	D27	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007A00	08E7D00000	FD5	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007B00	01B8700000	30F	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007C00	0032A00000	5A	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007D00	0038400000	64	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007E00	0593A00000	9EA	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	007F00	0325800000	598	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	008000	02FF400000	554	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	00	008100	05F5800000	A98	<input type="checkbox"/>	<input type="checkbox"/>

LPN	Address
00000000	035B800000
00000001	035B802400
00000002	035B804800
00000003	035B806C00
00000004	035B809000
00000005	035B80B400
00000006	035B80D800
00000007	035B80FC00
00000008	035B812000
00000009	035B814400
0000000A	035B816800
0000000B	035B818C00
0000000C	035B81B000
0000000D	035B81D400
0000000E	035B81F800
0000000F	035B821C00
00000010	035B824000
00000011	035B826400
00000012	035B828800
00000013	035B82AC00
00000014	035B82D000
00000015	035B82F400
00000016	035B831800
00000017	035B833C00
00000018	035B836000
00000019	035B838400

Blocks have been properly reorganized according to the logical block number (LBN)

File system reconstructed from NAND physical image

The screenshot displays the 'Visual Nand Reconstructor - solution' application. The interface includes a top toolbar with various actions like 'Check headers', 'Save image', 'Check file system', and 'Correct selected files data'. The main workspace shows a file tree for 'Volume0 (Microsoft NTFS) SSDv9 29.82 GB' under the 'Root' directory. A table lists the reconstructed files and folders with their names, extensions, sizes, and last modified dates.

Name	Ext	Size	Last modified
R251-275			06/07/2022 16:07:37
R276-300			06/07/2022 16:07:37
R301-325			06/07/2022 16:07:37
R326-350			06/07/2022 16:07:37
R351-375			06/07/2022 16:07:37
System Volume Information			06/07/2022 16:07:15
SAttrDef		2.50 KB	06/07/2022 16:07:13
SBadClus		29.82 GB	06/07/2022 16:07:13
SBitmap		954.09 KB	06/07/2022 16:07:13
SBoot		8.00 KB	06/07/2022 16:07:13
SLogFile		41.67 MB	06/07/2022 16:07:13
SMFT		256.00 KB	06/07/2022 16:07:13
SMFTMirr		4.00 KB	06/07/2022 16:07:13
SSecure		257.84 KB	06/07/2022 16:07:13
SUpCase		32 bytes	06/07/2022 16:07:13
SVolume		0 bytes	06/07/2022 16:07:13
autorun	ico	152.55 KB	01/07/2022 09:47:16
AUTORUN	INF	44 bytes	01/07/2022 09:47:34
EVENTLOG	TXT	128.00 KB	01/07/2022 09:47:14
mfc100	dll	4.19 MB	01/07/2022 09:47:20
msvcr100	dll	755.83 KB	01/07/2022 09:47:08
NTFS	EXE	952.50 KB	01/07/2022 09:47:28
xFULL-F	txt	256 bytes	06/07/2022 16:07:33
xQUICK-F	txt	256 bytes	06/07/2022 16:07:36

We have been able to successfully reconstruct file system for this SSD, and solution should generally work on all devices with same controller, NAND and capacity.

File system reconstructed from NAND physical image

The screenshot displays the 'Visual Nand Reconstructor - solution' application. The interface includes a top toolbar with various actions like 'Check headers', 'Save image', 'Check file system', and 'Correct selected files data'. The main workspace shows a file tree for 'Volume0 (Microsoft NTFS) SSDv9 29.82 GB' under the 'Root' directory. A table lists the reconstructed files and folders with their names, extensions, sizes, and last modified dates.

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SMFT		256.00 KB	06/07/2022 16:07:13
SMFTMirr		4.00 KB	06/07/2022 16:07:13
SSecure		257.84 KB	06/07/2022 16:07:13
SUpCase		32 bytes	06/07/2022 16:07:13
SVolume		0 bytes	06/07/2022 16:07:13
autorun	ico	152.55 KB	01/07/2022 09:47:16
AUTORUN	INF	44 bytes	01/07/2022 09:47:34
EVENTLOG	TXT	128.00 KB	01/07/2022 09:47:14
mfc100	dll	4.19 MB	01/07/2022 09:47:20
msvc100	dll	755.83 KB	01/07/2022 09:47:08
NTFS	EXE	952.50 KB	01/07/2022 09:47:28
xFULL-F	txt	256 bytes	06/07/2022 16:07:33
xQUICK-F	txt	256 bytes	06/07/2022 16:07:36

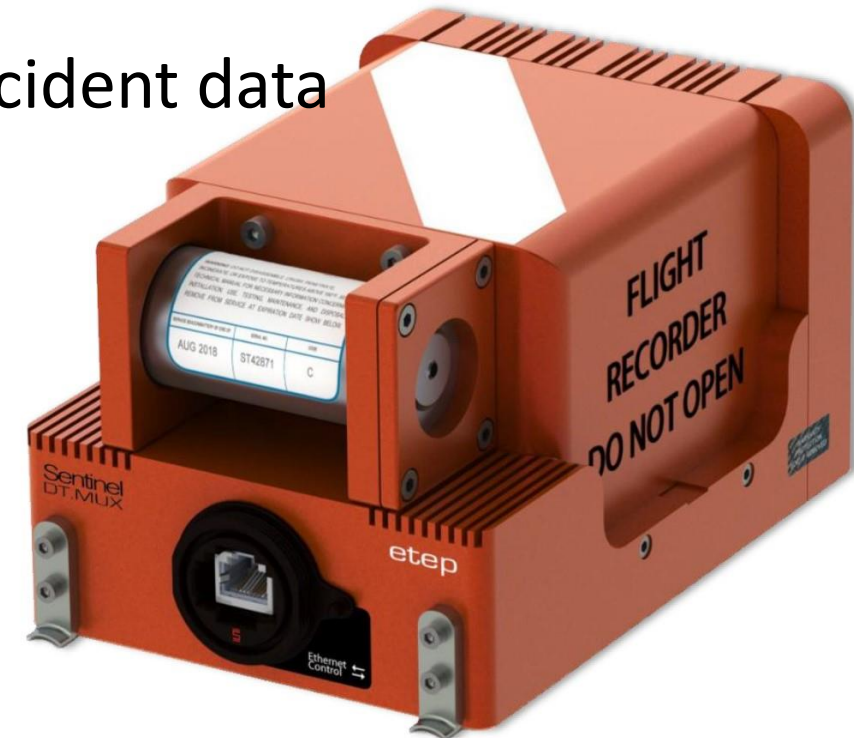
We have been able to successfully reconstruct file system for this SSD, and solution should generally work on all devices with same controller, NAND and capacity.

Conclusion:

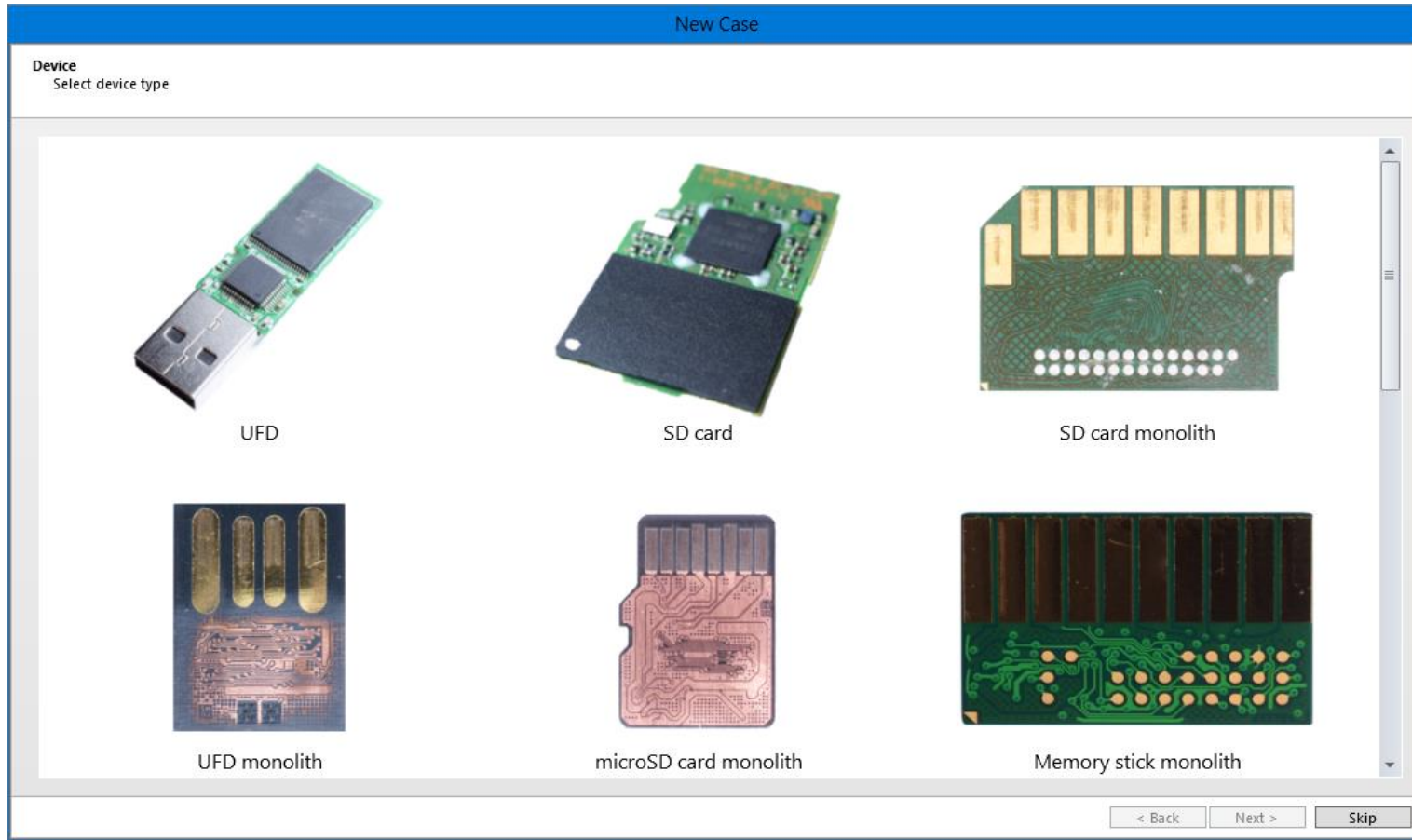
The SLC memory chip used in this device is very reliable. Even in the critical scenario of thermal damage, there's still high chance of successful data recovery. As long as memory chip is not cracked physically, the flight recorder is failproof.

Controller's data translation algorithm was fully reverse engineered and logical image was reconstructed.

It can be fed to the vendor's software for the flight accident data extraction.



Database of Solutions



- Integrated into VNR
- Dynamically updated
- Local, with Cloud sync
- Automatically adjustable solutions

Database of Solutions

New Case

Controller
Select controller model

Find controller

Filter controllers by vendor

- AlcorMicro(AU)
- Black blob
- Chipsbank(CBM)
- FirstChip(FC)
- Indilinx(IDX)
- Innostor(IS)
- Intel
- ITEtech(IT)
- JMicron(JM)
- Marvell(88SS)
- Other
- Phison(PS)
- Samsung
- SanDisk
- SiliconMotion(SM)
- Skymedi(SK)
- SolidStateSystem(SSS)
- Toshiba(TC)


AU_universal	AU6986	AU6987	AU6989ANHL
AU6989SN	AU6989SNCS	AU6989SNHL	AU6990
AU6998SN	AU69xx	Black blob 1	Black blob 2
Black blob 3	Black blob 4	Black blob 5	Black blob 6
Black blob 7	Black blob 8	Black blob 9	CBM_universal
CBM2098E	CBM2099	CBM2199	FC_universal
FC1178	FC1179	FC1250-TC-AL	FC1610-TC-AL
FC8708-C	IDX_universal	IS_universal	IS817
IS902	IS903	IS916	IS916EN

< Back Finish Skip

Database of Solutions

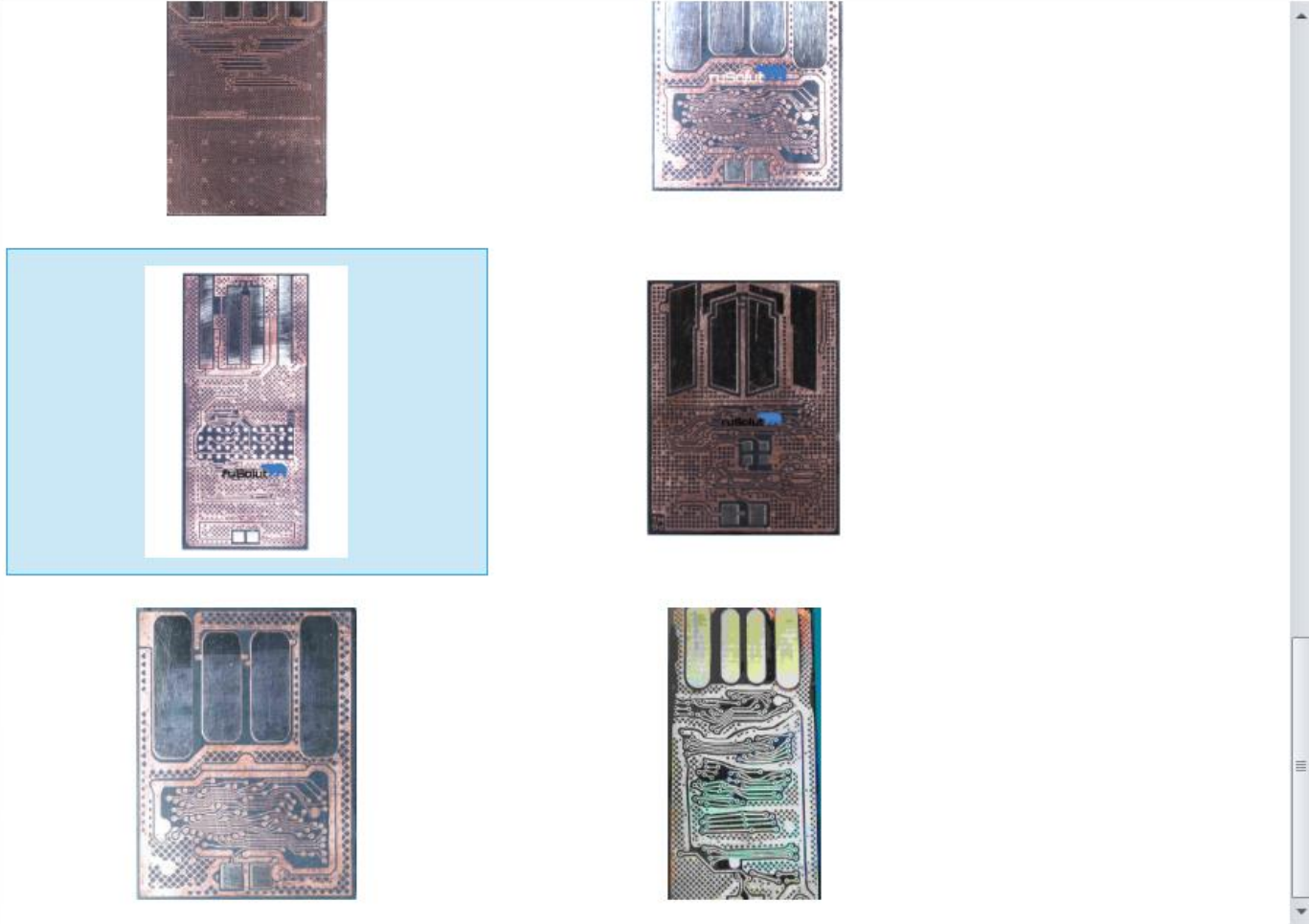
New Case

Monolithic device
Select monolithic device

Filter monolithic device by memory chip ID
  Read ID

Filter monolithic device by vendor

- Apacer
- CENTON
- Freecom
- Generic
- GoodRAM
- Hama
- HEMA
- Integral
- Intenso
- Kingston
- Lexar
- no name
- Other
- Panasonic
- Platinum
- pqi
- Pretec
- Samsung
- Sandisk
- Sony
- SP
- Toshiba
- Transcend
- Verbatim



< Back Next > Skip

Database of Solutions

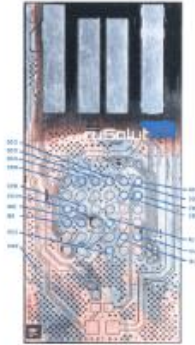
New Case

Monolithic pinout adapter

Insert chip into reader by means of adapter

Description

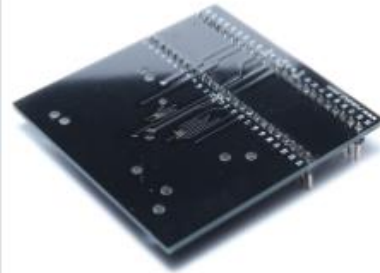
Pinout 0043



Adapter assembly

PCB

monoUFD 6x6



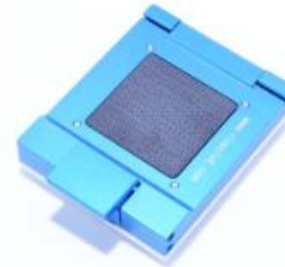
Frame

6x6 pads

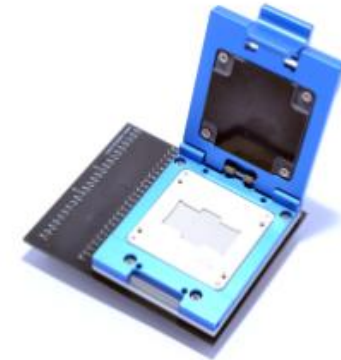


Socket

MONOUFD 6x6 & 3x7



Assembled adapter

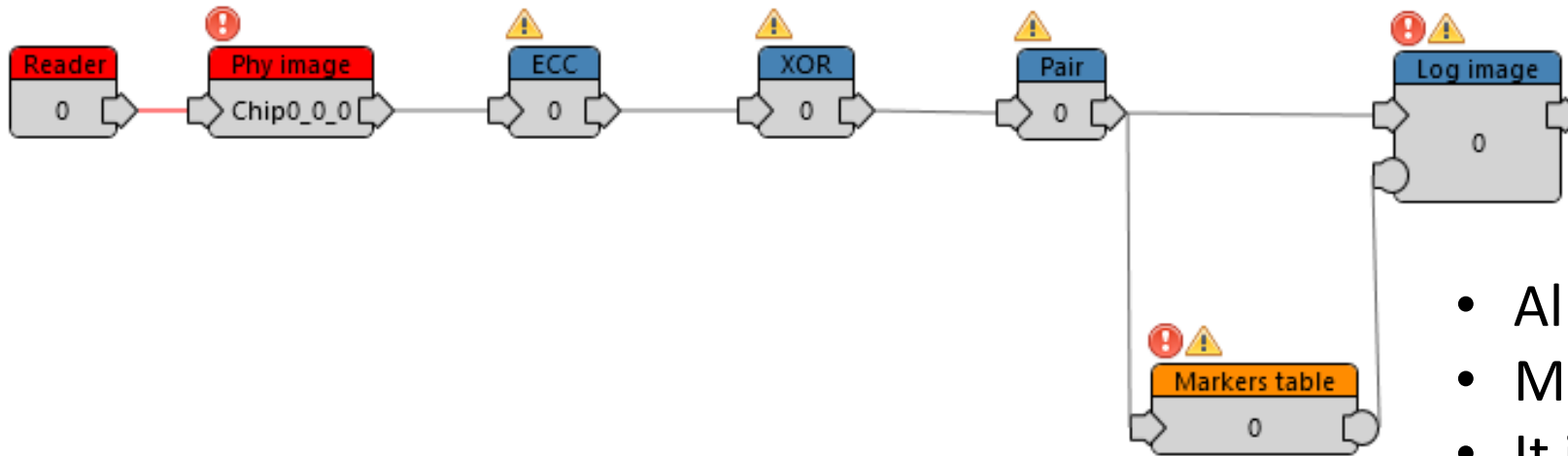


< Back

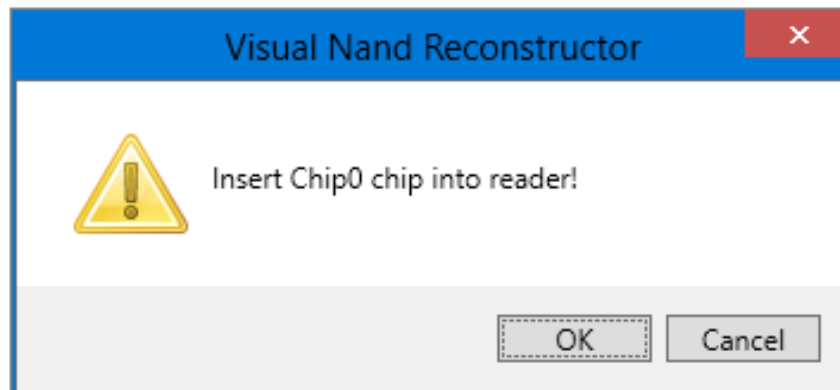
Finish

Skip

Database of Solutions – Full solution



- All parameters are defined
- Markers table is fully set up
- It is necessary just to read a chip and run the reread to fix bit errors



Thank you!